STUDY OF SOLID-STATE INTEGRATED MICROWAVE CIRCUITS

Scientific Report No. 5

U27-811500-27

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TEXAS INSTRUMENTS
INCORPORATED

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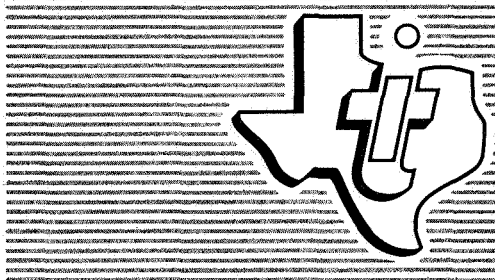
Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Electronics Research Center
Cambridge, Massachusetts



Work Performed Under
Contract No. NAS 12-75
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ABSTRACT

A study of the design techniques employed to develop a telemetry transmitter is presented.

Separate sections of the report present the circuit analysis and design of the individual blocks in the transmitter, the laboratory work, and thermal packaging considerations. The appendix includes the computer program written for the bandpass filter design and the transmitter test plan.

PREFACE

A study of solid-state integrated microwave circuits, under the sponsorship of the Electronics Research Center of the National Aeronautics and Space Administration, is being performed by Texas Instruments Incorporated under Contract NAS 12-75. The objective of this contract is to design and develop two thin-film, hybrid, breadboard telemetry transmitters. The models will not be integrated in a single substrate, necessarily, but may be of multiple chip construction, using up to three individual chips interconnected by conventional techniques.

This report presents the results of the design and development work performed under the sixth and seventh items in the work statement. The period covered is 15 December 1966 through 14 June 1967. The sixth task is concerned with a detailed test and evaluation plan for the breadboard transmitter, based on the results of item five. The seventh task is concerned with the fabrication of two breadboard models of the specified integrated telemetry transmitter subsystem, exclusive of AFC circuitry, and based on the results of item five.

Separate sections of the report present a description of the system, detailed circuit design and analysis of individual blocks in the transmitter, laboratory work, and thermal packaging considerations. The appendix includes a computer program for the design of bandpass filters and a system test plan.

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SECTION I

INTRODUCTION

Integrated circuits constitute a very significant part of the burgeoning domain of microelectronics. As a result of their proven advantages in size and reliability these circuits have come to be preferred for use in military and space applications. Recently, developments resulting in the added advantages of lower cost and higher performance have made such devices practical and competitive for commercial, industrial and consumer applications also. This progress has brought integrated circuit technology to the point where operation of linear integrated circuits in the microwave-frequency range now appears feasible, even though special techniques and circuits are required.

A study program was undertaken to establish the feasibility of employing integrated circuit techniques at microwave frequencies. The first phase, completed on 15 December 1965, was a three-month study of solid state microwave devices, techniques and components suitable for use in the 1- to 6-GHz frequency range, and their application to integrated circuitry. Investigated during the second phase were basic FM telemetry transmitter configurations suitable for use in the 1- to 6-GHz frequency range and for implementation in integrated circuits; this three-month study was completed on 14 March 1966. During the third phase, nine months long and completed on 14 December 1966, the final transmitter configuration was selected. Detailed design and analysis of the transmitter was completed, along with a study of computer-aided circuit design techniques and the effects of radiation on integrated circuits.

This report covers the period from 15 December 1966 through 14 June 1967. During this six-month period the breadboard development was initiated for the telemetry transmitter without the AFC circuitry. The requirements for the transmitter are those normally associated with earth-space telemetry systems:

Frequency	1.7 to 2.3 GHz (fixed)
Frequency stability	±0.5% (without AFC circuitry)
Modulation	
Type	FM and/or FSK
Linearity	1% for FM
Baseband	2 kHz to 1 MHz
Sensitivity	0.2 volt rms/100 kHz
Deviation	±1.5 MHz
Input impedance	600 ohms
Output impedance	73 ohms

Power output	1.0 to 5.0 watts
DC input	-24.5 volts
Efficiency (dc to RF)	10 to 20%
Size	Approximately 6" x 2" x 6-1/2"
Weight	Approximately 4 pounds

In conjunction with the breadboard, work was also started on device characterization, matching network design, bandpass filter design, and thin-film circuit development. A system test plan was completed.

SECTION II

SUMMARY OF RESULTS

The circuit analysis and design of the breadboard transmitter was completed. The design of the Teflon board oscillator was also completed and a ceramic layout was started. In order to minimize the fabrication time of the oscillator and realize a ceramic chip that would be as small as possible, chip capacitors were used and two quarter-wavelength lines were removed. The actual circuit area is 300 by 320 mils, including a 10-mil border. The Teflon circuit produces a power output of 117 to 147 mW across the 100-MHz band (2200 to 2300 MHz), corresponding to an attenuation of 0.845 dB. The oscillator was capable of tuning 545 MHz (1912 to 2457 MHz) with a power output of 64 to 58 mW at the end points. The initial oscillator was subjected to a temperature environment of -28° to 71°C with a resulting frequency change of 18.2 MHz (±0.40 percent).

The dissipation tests conducted on the L-158A devices indicated that the L-158A could not produce a 1-watt RF output using a collector supply voltage of 24 volts dc. As a result, a parallel amplifier configuration was selected. Having established the power output requirement of the final stages of the amplifier (540 mW per path), device characterization proceeded.

Using the characterization test results, input, output, and interstage matching networks were designed, using an efficient computer program. After fabrication, tests conducted on these networks indicated an error in the computer program. This error was corrected and the networks were redesigned.

Because of the parallel amplifier configuration, a network for splitting the power at the amplifier input and combining it at the output was necessary. The network, a combination N-way and reactive power divider, was designed and fabricated on Teflon-fiberglass. Test results indicated that the divider performance was adequate for our application—VSWR 1.3:1, isolation > 20 dB. The performance of the divider should improve when it is fabricated on ceramic because smoother transitions at its ports will be possible.

The entire power amplifier chain was layed out on Teflon-fiberglass and measures 6.58 inches by 1.39 inches. No attempt was made to optimize the size of the total layout although individual networks were optimized for size and theoretical performance.

In order to investigate device characteristics further, a ceramic test circuit, a test stand, and connectors were designed and fabricated. This test set will allow devices to be evaluated without the presence of package parasitics. As part of this investigation, a thermal analysis is proposed.

The multiplier output bandpass filter was optimized during the report period and yielded a 9-element (5 series elements, 4 shunt elements) filter which approaches the design goals. The final filter response resulted in midband insertion loss of 0.375 dB; the attenuation increases rapidly to 22.54 dB at 2.7 GHz and 29.95 dB at 1.8 GHz.

The actual size of the ceramic layout is 600 by 935 mils. This probably could be reduced if the elements were meandered more. To minimize coupling between elements, however, meandering was kept to a minimum.

SECTION III

SYSTEM DESCRIPTION

The system chosen to demonstrate microwave integrated circuit techniques during the third phase of this study was the gated discriminator AFC system, (Figure 1). The system performance will be reviewed in order to establish the baseline for the final system.

The gated discriminator AFC system is capable of performance significantly above that of a simple discriminator AFC system. The operation of the gated discriminator AFC is shown in Figure 2.

The square-wave generator alternately switches either the RF output frequency or the reference frequency into the limiter-discriminator for equal periods of time. Normally, in discriminator AFC systems, the discriminator center frequency is chosen as the desired output frequency. This is not necessary, however, in the gated system shown. In actual use the discriminator center frequency would be the center of the desired tuning range. Assume, then, that the discriminator center frequency f_d is different from the reference frequency f_r (Figure 2). The system functions to correct the discrepancy between the output frequency f_o and the reference frequency f_r by developing the associated voltages e_o and e_r at the output of the discriminator.

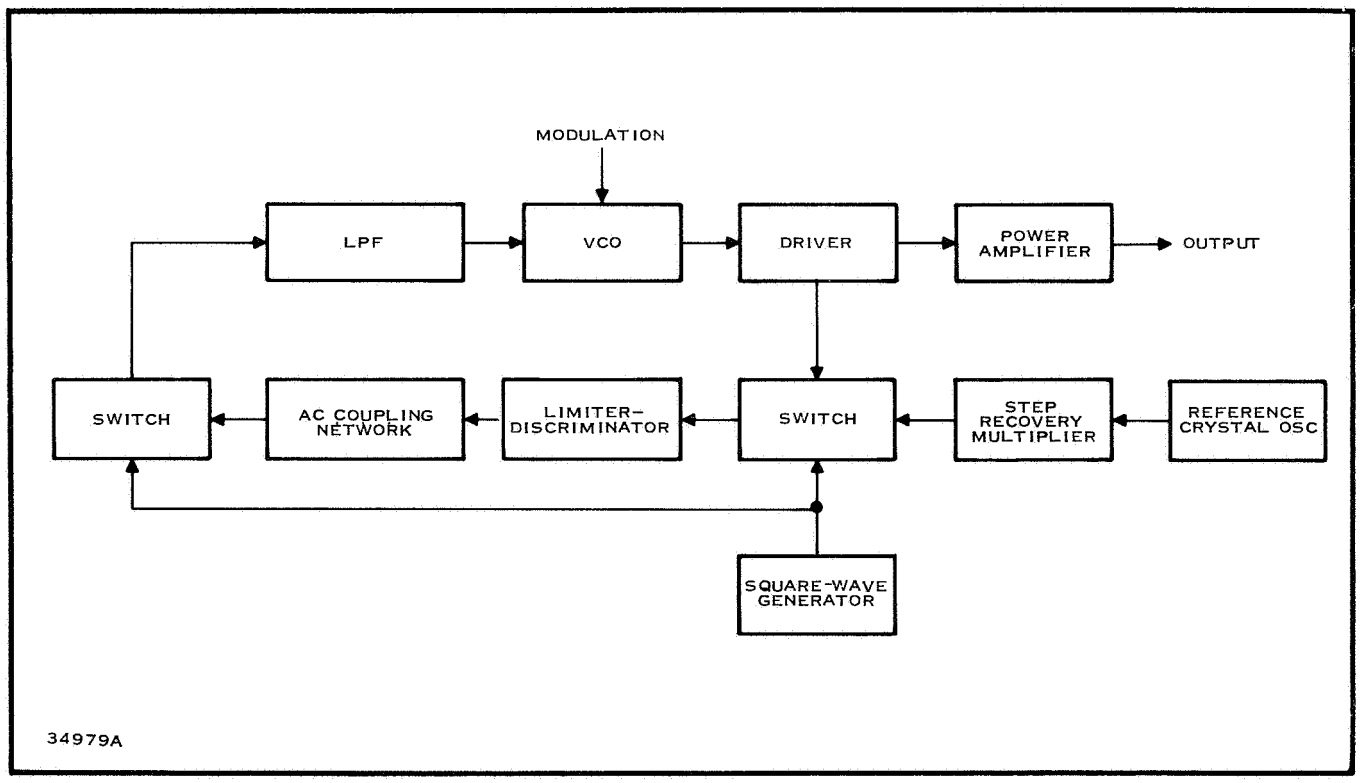

Figure 1. Gated Discriminator AFC-FM Transmitter

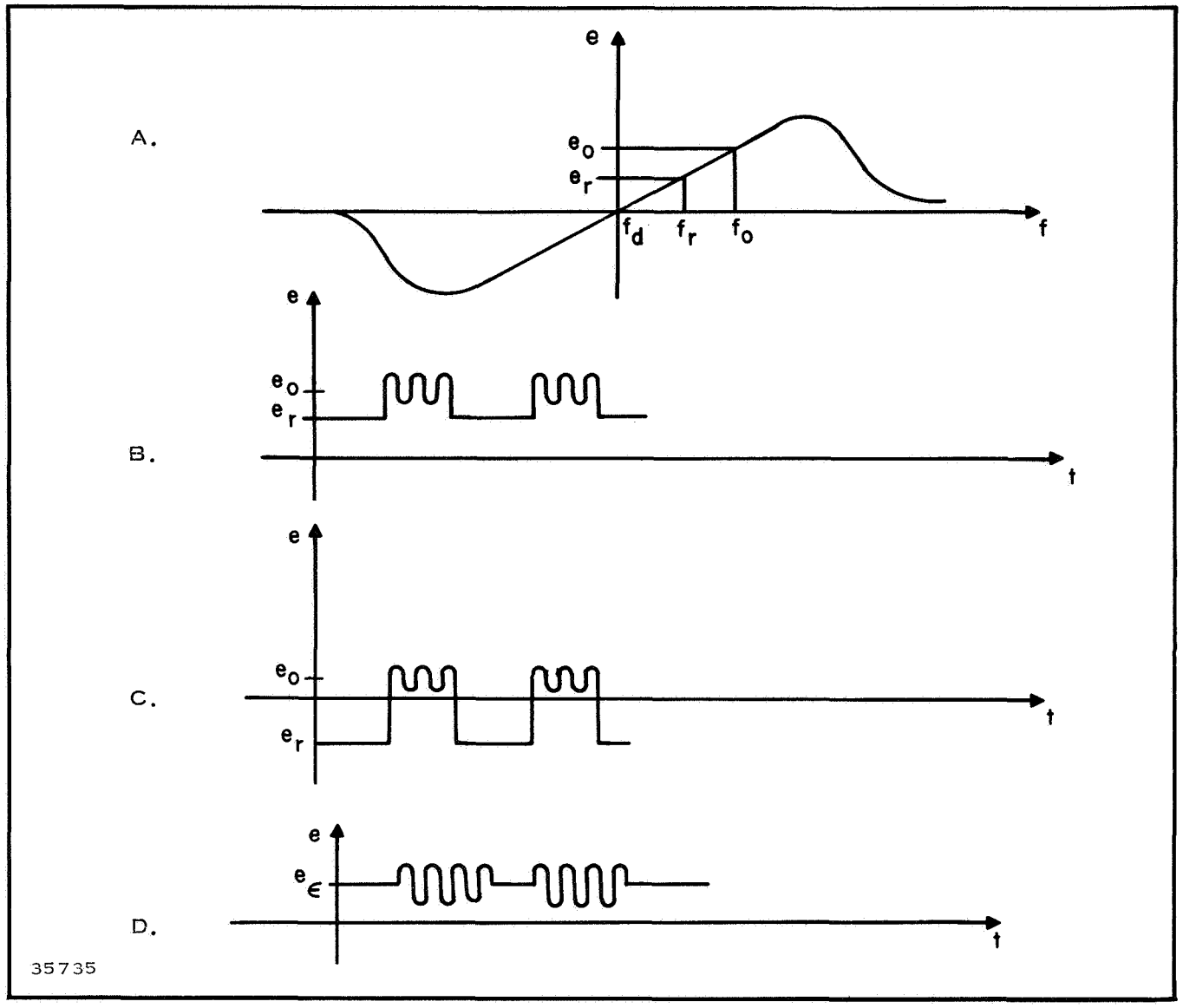

Figure 2. Gated Discriminator AFC-FM Transmitter

Figure 2 shows the time waveform resulting from the square-wave switching. The modulation is superimposed on the mean value of the output frequency and thus appears in the discriminator output. This signal cannot be used directly as an error signal because of the difference between f_d and f_r. If, however, the signal is simply ac coupled, the dc offset is removed. The signal is then synchronously demodulated by a second switch driven from the square-wave generator. The output of the demodulator is then passed through the low-pass filter and is applied to the VCO to correct the frequency offset. In the example shown, f_r is lower than f_o; had the reverse been true, the polarity of the error signal of Figure 2 would have been negative.

The final system selected to be built during the fourth and fifth phases is the gated discriminator AFC-FM transmitter, without an AFC system. The system will contain a modulator, voltage-controlled oscillator, and driver and power amplifier; it will meet the specifications as stated in the introduction and will be tested according to the detailed test plan in Appendix B.

SECTION IV

CIRCUIT DESIGN AND ANALYSIS

A. Voltage-controlled Oscillator

1. General

As one of the functional blocks in the AFC transmitter, the voltage-controlled oscillator was the first item fabricated under the existing contract. The initial developmental work used etched, copper clad, Teflon circuit boards, although the ultimate fabrication will use thin-film hybrid techniques and a ceramic substrate. Both of these techniques were considered during this phase.

The basic oscillator circuit chosen is, essentially, the Colpitts configuration. Figure 3 shows the lumped-constant equivalent circuit and the schematic of the modified Colpitts oscillator with varactor tuning. It is customary at microwave frequencies to use a semidistributed approach to realize the oscillator circuit. When a tuned quarter-wavelength line is used at the emitter to provide the emitter susceptance, the emitter-to-ground terminal capacitance of the active device can be taken into account. The length of the shorted stub can be set to provide the right susceptance valve at the emitter, in combination with internal feedback, to provide an optimum feedback divider network. A slightly more restrictive, but just as practical, way of realizing emitter susceptance is to use an emitter open circuit line or short. The collector tank circuit can also be realized with similar techniques.

2. Teflon Design

a. 3016A (SA9900) Oscillator

The initial oscillator design described in the Third Scientific Report was fabricated on Teflon board. The actual circuit layout was the same as reported in the Third Scientific Report but the type of device utilized was changed.

The original device, L-49 (7-stripe) had been changed to a 13-stripe device in order to achieve higher output power. The new device, designated SA9900, has a guaranteed minimum oscillator output of 100mW at 2GHz for 12 volts and 30 mA.

Initial tests with two SA9900 devices showed that the output frequency and power were less than expected. From this it was obvious that the 2-transistor configuration had characteristics different from those of the 3-transistor group (original design). Therefore, the design would have to be modified.

Initial test data (Figure 4) shows the output power versus frequency response of the oscillator. The varactor voltage necessary to obtain the required frequency response was 11.3 to 17.5 volts (2200-2300 MHz). The output power was not very smooth, as the devices were critically sensitive to emitter current.

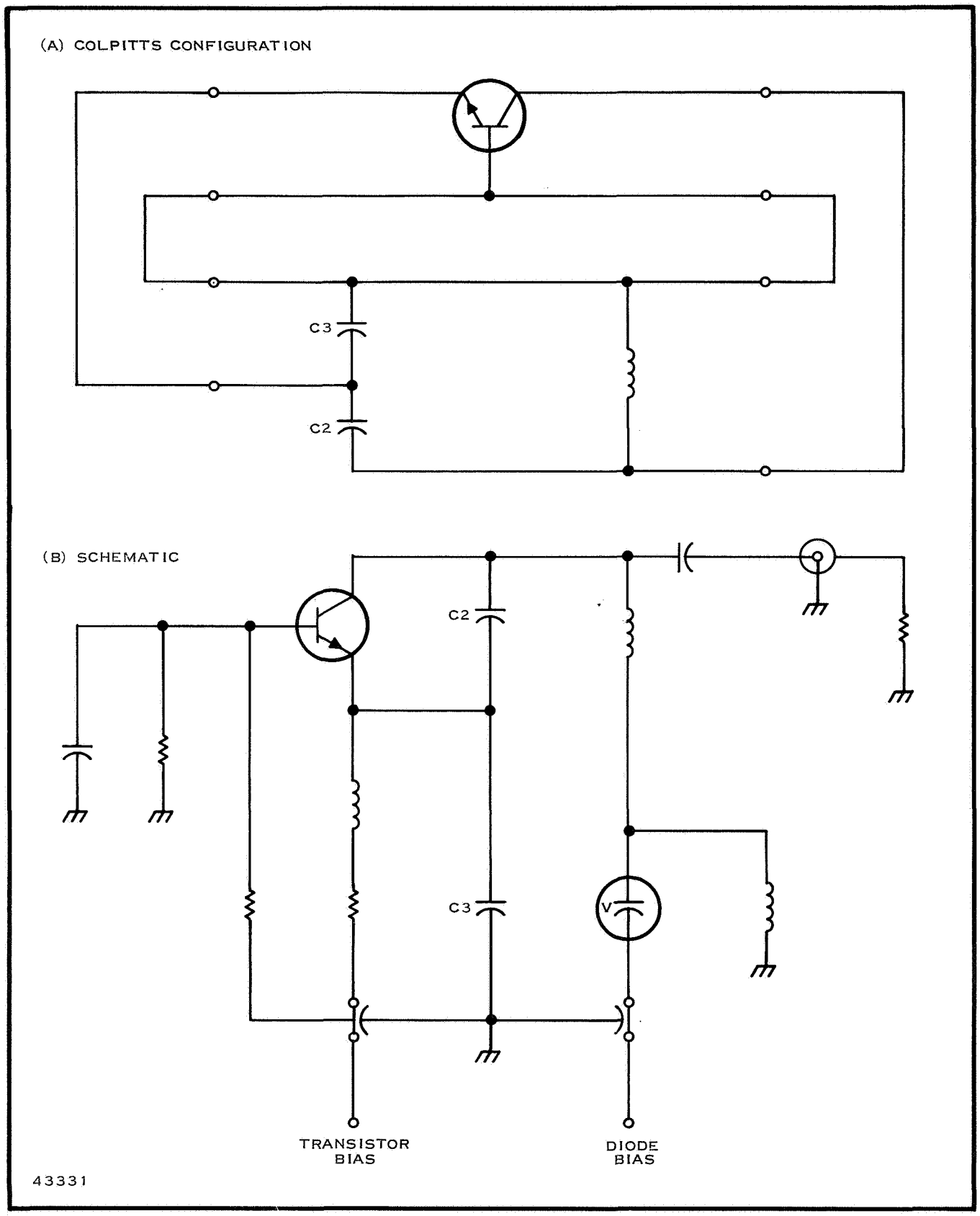

Figure 3. Colpitts Configuration

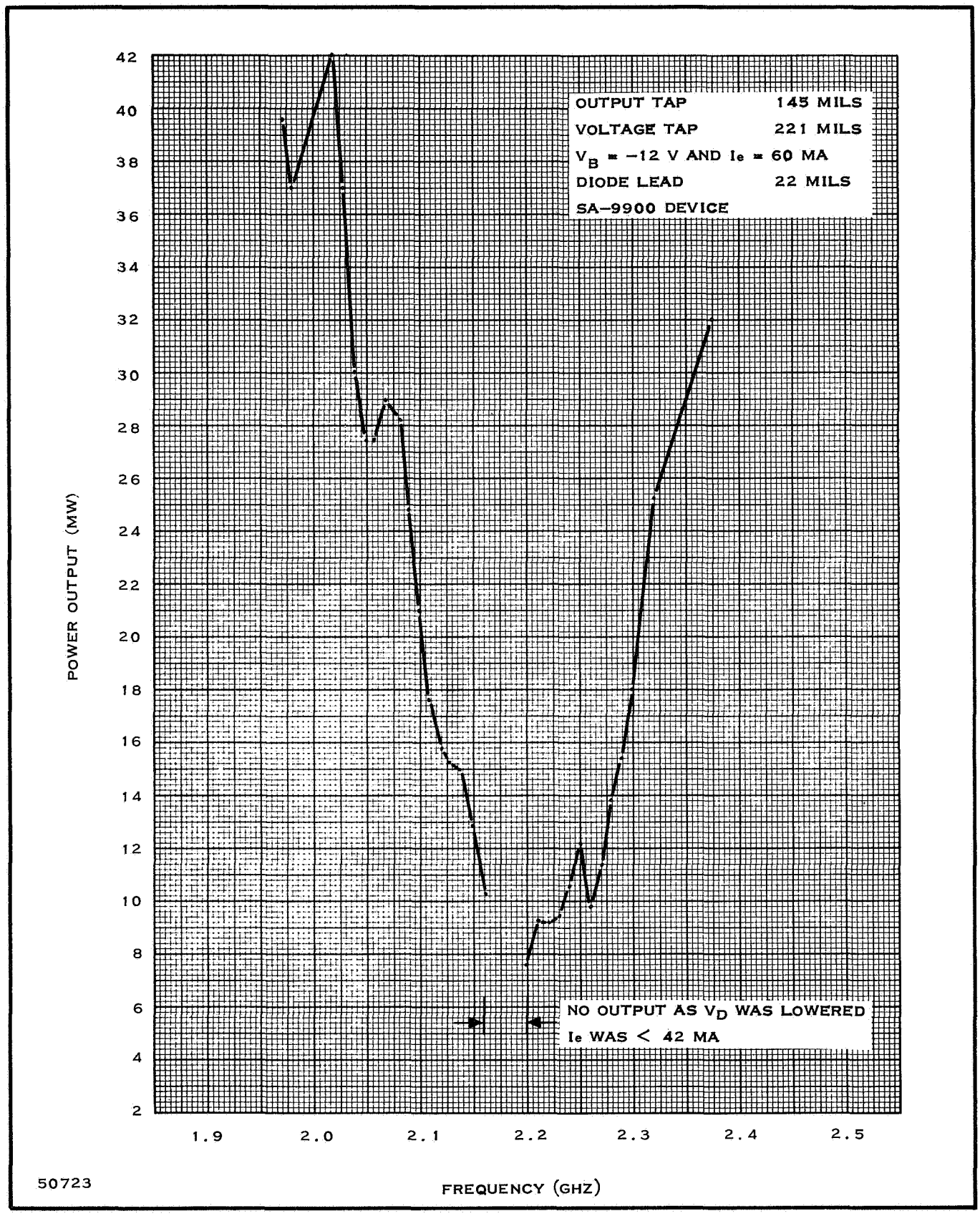

Figure 4. Initial Test Data

To obtain higher output power across the band the collector line was changed to resonate at 2.5 GHz. The resulting output power is shown in Figure 5. The big differences between the two curves are the smoothness of the second and the varactor voltage required to tune the frequency range. Figure 5 shows that a voltage swing from 5.7 to 8.8 volts was required to tune from 2200 to 2300 MHz.

The data may also be used to check the terminating susceptance on the transmission line.

At the null point of the voltage standing wave on the collector line the impedance is resistive and may be plotted along the axis of the Smith Chart. As the oscillator frequency is varied, the output power passes through a minimum, or null, which indicates that, at that particular frequency, the output tap position coincides with the voltage null. Since the physical location of the tap and the operating frequency are known, the terminating susceptances can be determined by rotating (from the Smith chart axis toward the terminating susceptance) the known distance from the tap point to the susceptance.

The null frequency of Figure 4, for example, is 2.2 GHz and one wavelength (λ) would be 3.89 inches. Rotating the fractional wavelengths from the tap point toward the generator and toward the load will yield the terminating capacitances. Figure 6 shows the measured terminating capacitances to be 3.03 and 0.75 pF, respectively, for the output capacitance of the device, C_t, and the capacitance of the varactor, C_j.

The same procedure was followed for the higher resonant frequency (Figure 5) and the value obtained for C_j was 0.653 pF while the value for C_T was 7.21 pF. The values are shown in Figure 6 (dotted line). Table I shows the terminating susceptances for the two cases, compared to the design values.

Table I

Terminating Susceptances

	Design (pF)	Measured (pF)	Frequency (GHz)
C_j	0.6	0.75	2.2
C_T	2.0	3.03	2.2
C_j	0.6	0.653	2.325
C_T	3.74	7.21	2.325

The differences in C_T are due mainly to parasitics and the constraints put on the tank circuit. The tank was designed to oscillate at 2.3 GHz with a minimum junction capacity not chosen at a maximum voltage. Therefore, to oscillate over a 100 MHz band would require a small change in varactor voltage, which is difficult to achieve. The null locations on the collector line are so close in this case that the frequency cannot be shifted to any great extent.

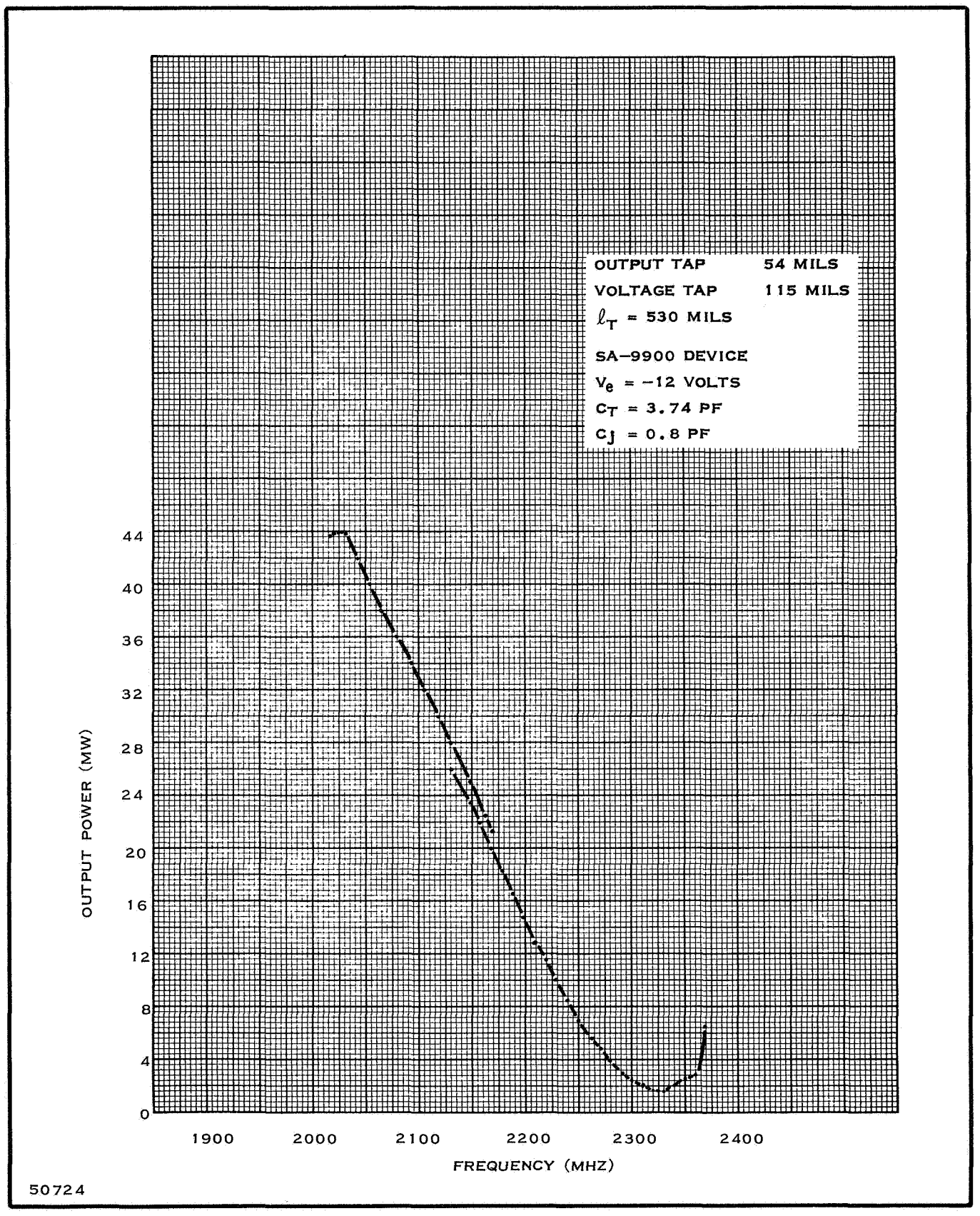

Figure 5. Power Output Versus Frequency

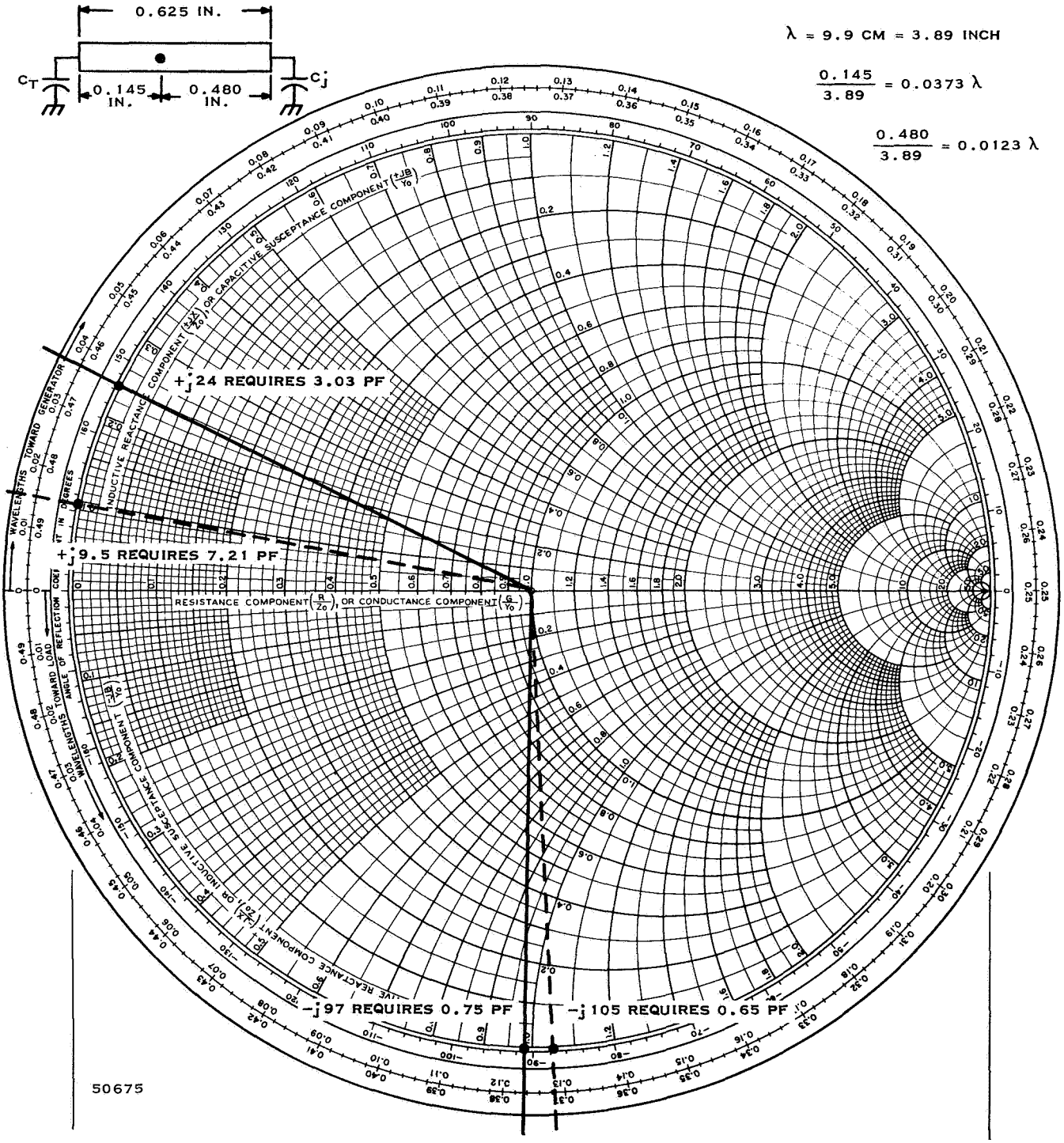

Figure 6. Terminating Susceptances

The starting conditions were another problem affecting the output power. The oscillator required 56 mA for output frequency detection; if the current were less, the spectrum had many components that were of approximately the same amplitude, allowing only the difference frequency to be detected on a counter.

To alleviate the previously mentioned problems, a new design was prepared. The design took into account the starting conditions. The frequency range was opened to 2.5 GHz and the minimum varactor capacitance was used for the maximum voltage available. This allows freedom in choosing the best varactor voltage to achieve maximum power output in the band of interest.

The basis for the design of the feedback circuit of any oscillator is the characteristic equation of the complete circuit. Evaluation of its real part reveals the starting conditions, whereas a solution for the imaginary part shows the expression for the resonant frequency. It may be shown (Section IV.D.2 of the Third Scientific Report) that the starting conditions are satisfied if the condition in Figure 7 is met.

The component C_2 is the total (external and internal) effective capacitance from collector to emitter and C_1 is the total effective capacitance from emitter to ground. Note that neither of these capacitors necessarily needs to be external to the transistor. For a given set of conditions (bias, frequency, transistor, et cetera) power output will be maximized by a specific ratio of $C_2/(C_1 + C_2)$. Since h_{fb} obviously is a function of frequency, its exact value is determined experimentally.

In order to redesign the VCO, the output capacitance of the device and the emitter-to-collector capacitance must be determined. These data are difficult to obtain for a chip device but for a packaged device the output capacitance and the emitter-to-base capacitance are known. Recent work on the different types of transistor packages has yielded their characteristics, making design work with chip transistors easier.

Data on the SA9900 device shows that the output capacitance is 1 pF for a collector-to-base voltage of 12 volts. Allowing 0.4 pF capacitance for the package output yields an output capacitance of 0.6 pF for the chip. The emitter-to-base capacitance (input capacitance) is 3.5 pF for 0.5 volts emitter-to-base voltage. Allowing 0.5 pF for the package input capacitance yields a chip capacitance of 3.0 pF.

The starting conditions, as stated previously, must be satisfied, and in order to arrive at them the value of the emitter-to-collector capacitance is required. A high frequency T equivalent circuit for a junction transistor is shown in Figure 8. C_e is the emitter-junction capacitance which, at high frequencies and low emitter currents, reduces the emitter efficiency. In many cases it may be neglected, in comparison to the emitter diffusion capacitance C_e'.

The emitter diffusion capacitance is given by

$$C_e' = \frac{0.81}{W_\beta \, r_e'} \qquad (1)$$

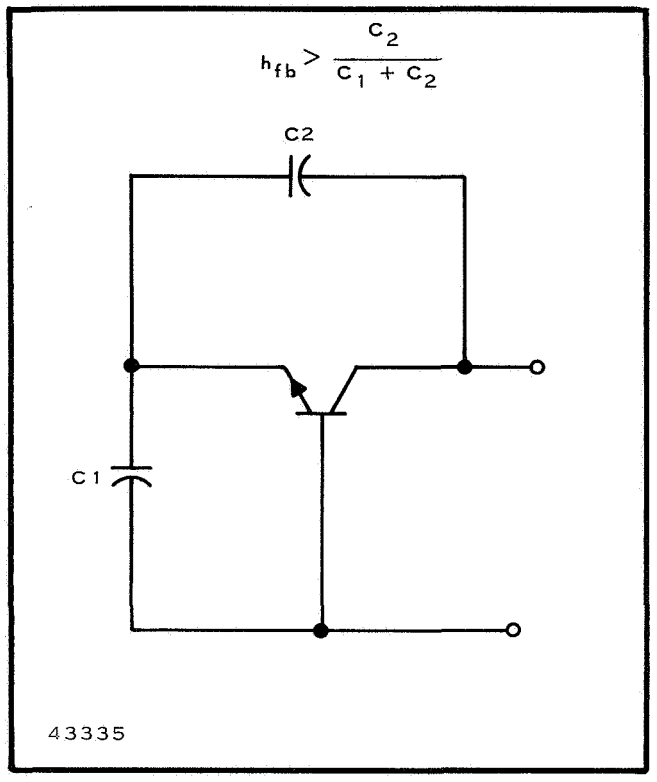

Figure 7. Starting Conditions

where W_β is the β cutoff frequency and is defined by

$$W_\beta = 2.43/\tau d = 2.43 \left[D_x/W^2\right] = k/\tau d \quad (2)$$

k is approximately equal to the total low-frequency common-base current amplification factor α_o.

D_x = diffusion constant, cm^2/sec

W = base width, cm

τd = diffusion time of minority carriers

r'_e = input resistance

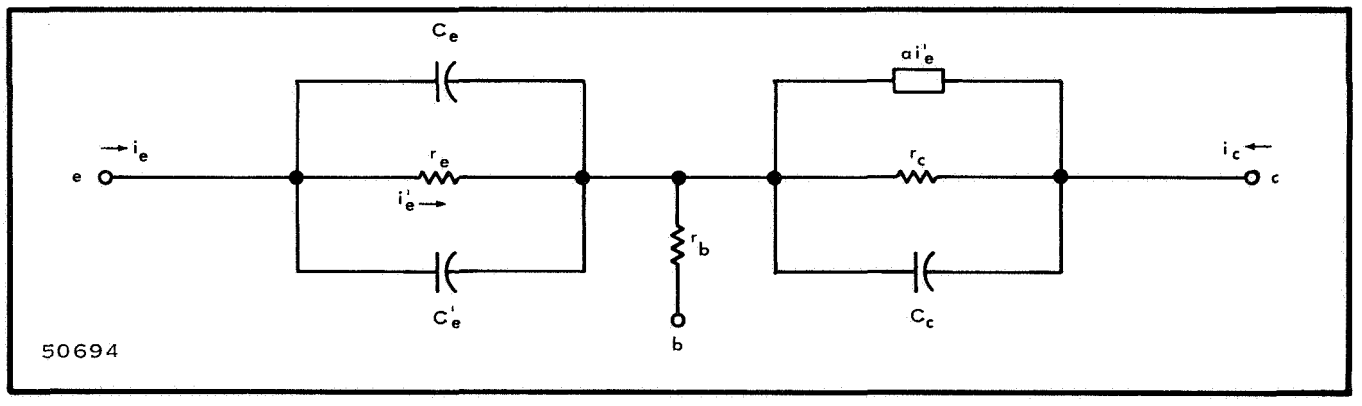

Figure 8. High Frequency T Equivalent Circuit

It is now possible to calculate the emitter-to-collector capacitance.

$$W_\beta = \frac{2.43 \times 34}{(2.54 \times 10^{-5})^2}$$

$$W_\beta = 12.8 \times 10^{10} \tag{3}$$

Therefore:

$$C_e' = \frac{0.81}{12.8 \times 10^{10}\, r_e'} \tag{4}$$

but

$$r_e' = \frac{kT}{QI_e} = \frac{26mV}{I_e} \tag{5}$$

where

K = Boltzmann's Constant, 1.38×10^{-16} erg/^oK

T = Temperature, ^oK

Q = Charge on the electron, 1.6×10^{-19} coulomb

$\therefore$ Ie = Emitter current, in mA

$$r_e' = 26/30 \tag{6}$$

$$r_e' = 0.866 \text{ ohm}$$

and

$$C_e' = 7.3 \text{ pF}$$

The emitter-to-collector capacitance can now be obtained by adding the diffusion capacitance with the collector capacitance.

Therefore:

$$C_{ec} = C_e' \parallel C_{ob}$$

$$= 7.3(0.6)/7.3 + 0.6 \tag{7}$$

$$= 4.38/7.9$$

$$C_{ec} = 0.555 \text{ pF}$$

To calculate the starting condition the value of h_{fb} must be known. In order to arrive at a value for h_{fb} the y parameters must be calculated. The data available on the SA9900 series only go to 1 GHz, therefore, the curves have to be extrapolated. From the extrapolated data curves, values of y_{ib} and y_{fb} at 2.3 GHz were found to be:

$$y_{ib} = -42.8 + j35.7 = 55.7 \angle 39.8° \text{ mmhos}$$

$$y_{fb} = 0 - j32.2 = 32.2 \angle -90° \text{ mmhos}$$

and since h_{fb} equals y_{fb}/y_{ib}

$$\left| h_{fb} \right| = 0.576$$

Since the two transistors are in parallel, the value of C_2 will be 2(0.555) or 1.11 pF. Applying this value to the starting conditions yields

$$h_{fb} > \frac{C_2}{C_1+C_2}$$

$$0.6 = \frac{1.11}{C_1+1.11} \qquad (8)$$

$$0.6C_1 + 0.666 = 1.11$$

$$C_1 = 0.74 \text{ pF}$$

This is the total capacitance from emitter to base, and, for the inequality to be satisfied, C_1 must be greater than 0.74. The optimum value is usually two to four times this value; a value of 2 pF was assumed.

The length of the emitter tab will be

$$l = VZC$$

$$= \frac{3 \times 10^{10}}{1.38} \times 40 \times 2 \times 10^{-12}$$

$$= \frac{2.40}{1.38}$$

$$= 1.74 \text{ cm}$$

$$l = 685 \text{ mils}$$

The tank circuit analysis is made by assuming a terminating capacitor value and investigating the tank and diode constants required to obtain a given tuning range.

Using the value obtained from the data sheets for the SA9900, the output capacitance C_{ob} would be 0.6 pF per device or 1.2 pF total. Since this is in parallel with the feedback capacitor it must be accounted for. Figure 9 shows the feedback arrangement:

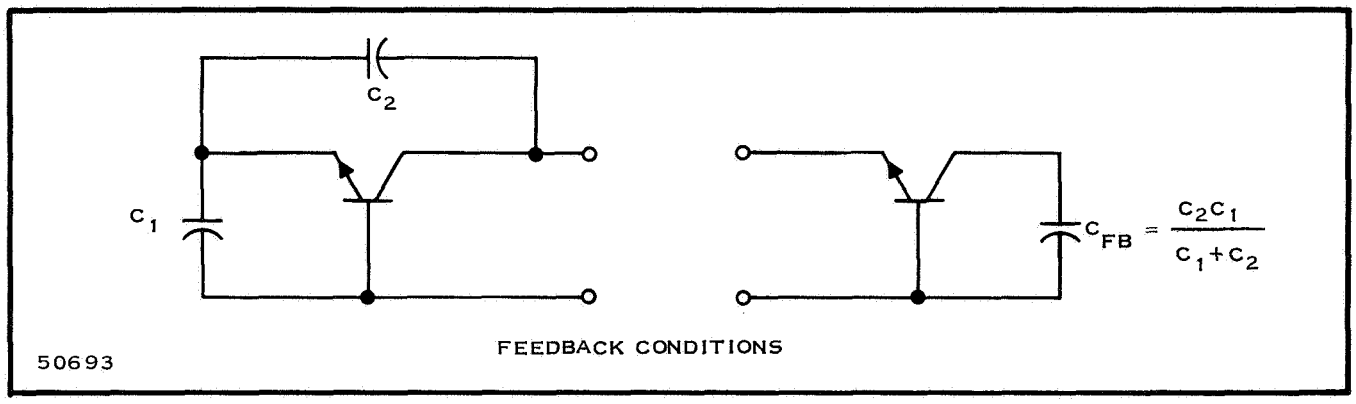

Figure 9. Feedback Conditions

From the figure it can be seen that a value of C_T can be obtained as follows

$$C_T = C_{ob} + C_{FB}$$

For two devices C_{ob} must be multiplied by two, therefore

$$C_T = 2C_{ob} + C_{FB} \quad (2)$$

$$= 2(0.6) + \frac{C_2C_1}{C_1 + C_2} \quad (2)$$

$$= 1.2 + \frac{1.11\ (0.74)}{1.11 + (0.74)} \quad (2)$$

$$= 1.2 + 0.613$$

$$C_T = 1.813 \text{ pF}$$

The tank circuit can be calculated from either the Smith Chart or the computer print out as follows: The calculations will assume a C_T of 2 pF and a varactor capacitance of 0.46 pF at 20 volts bias (Figure 10). Using Figures 11 and 12, tank antiresonant frequency for C_{jmin} of 0.4 pF and 0.5 pF, it can be seen that at 2.2 and 2.3 GHz the capacitances required would be between 0.57 and 0.68 pF and between 0.69 and 0.83 pF, respectively. Taking the average values for the two cases the desired capacitances required to tune from 2.2 to 2.3 GHz will be approximately 0.6325 pF (11 volts) and 0.755 pF (7.5 volts).

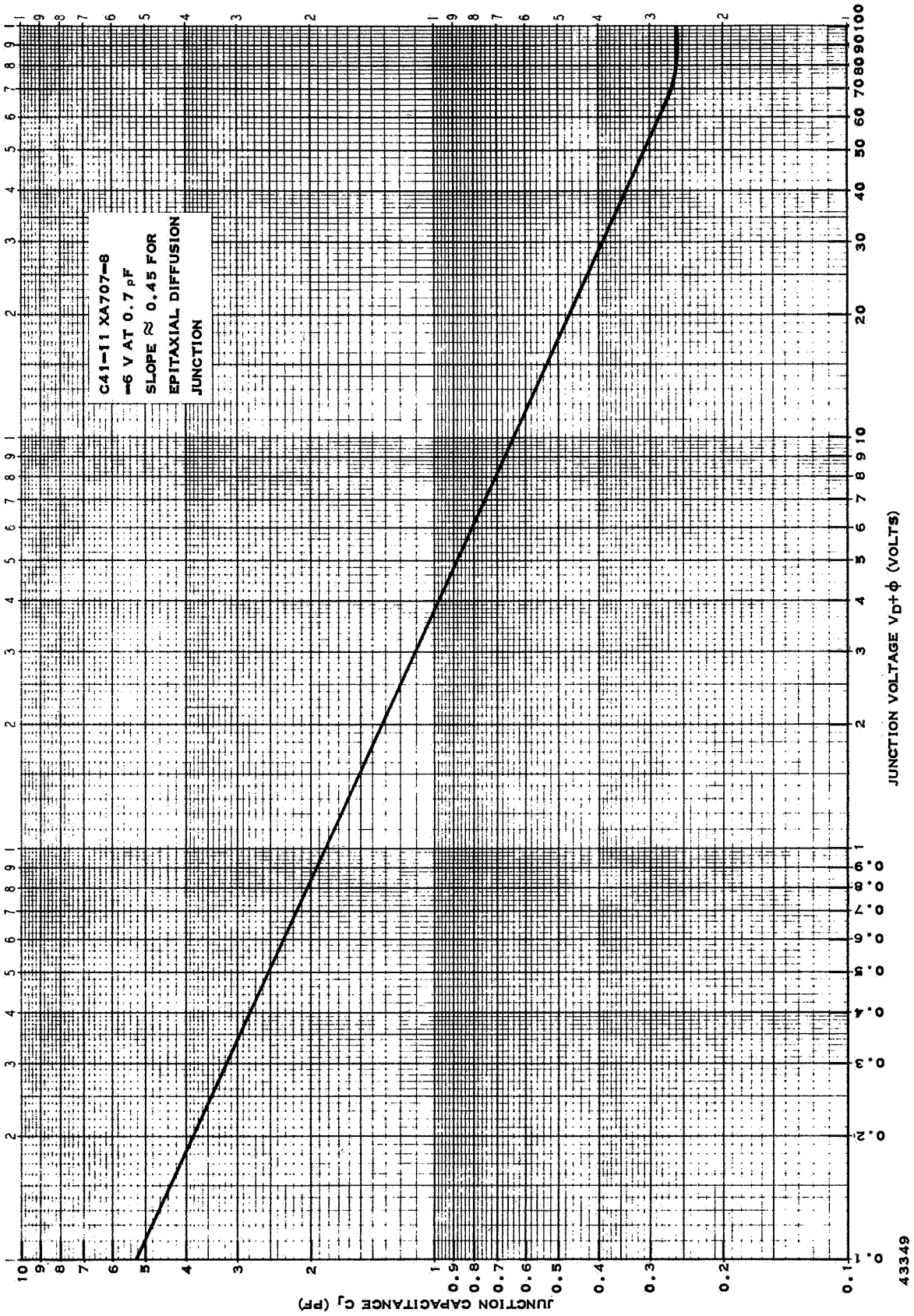

Figure 10. Varactor Capacitance Versus Voltage

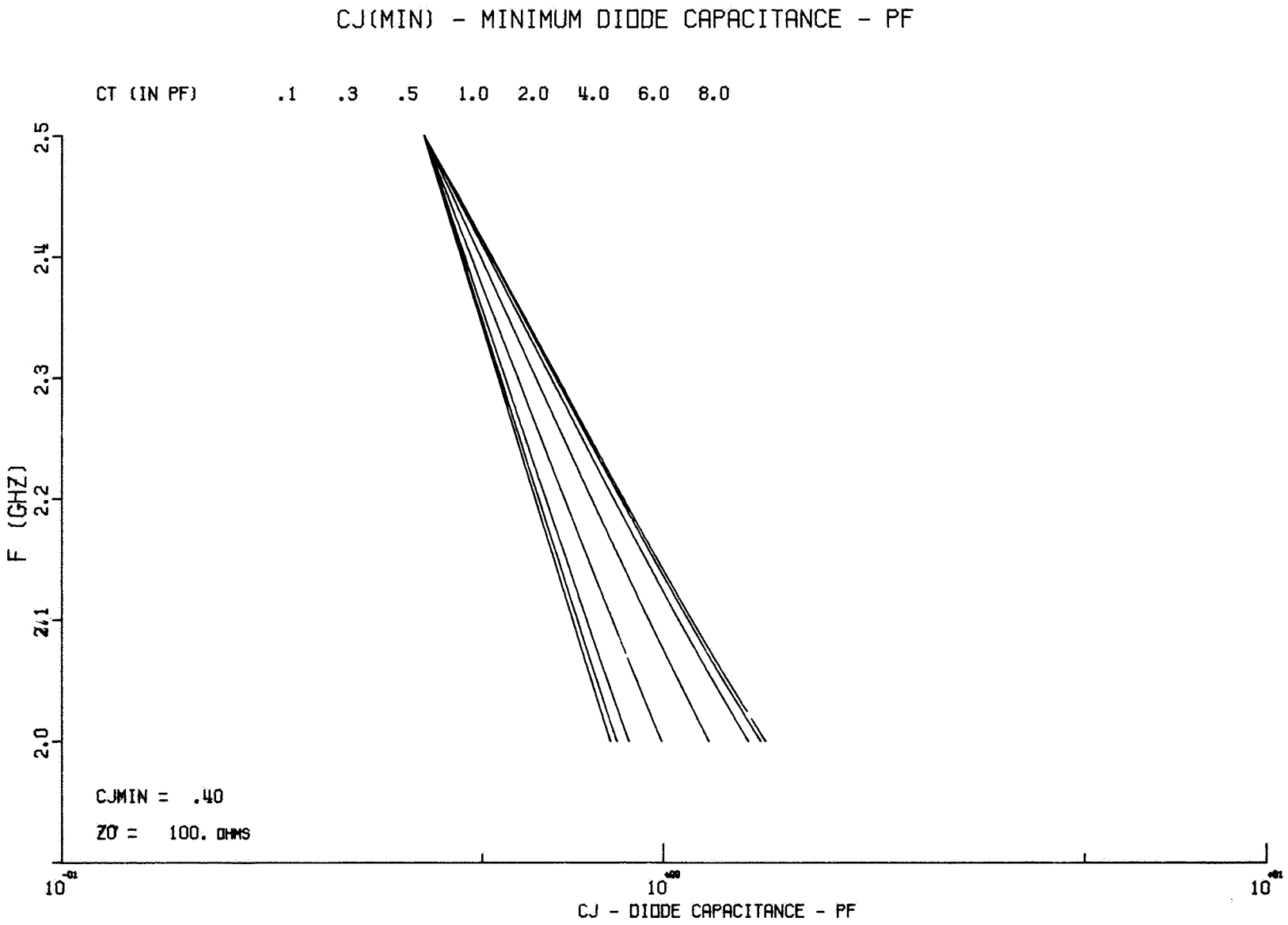

Figure 11. Tank Antiresonant Frequency Versus Diode Junction Capacitance with C_T as a Parameter

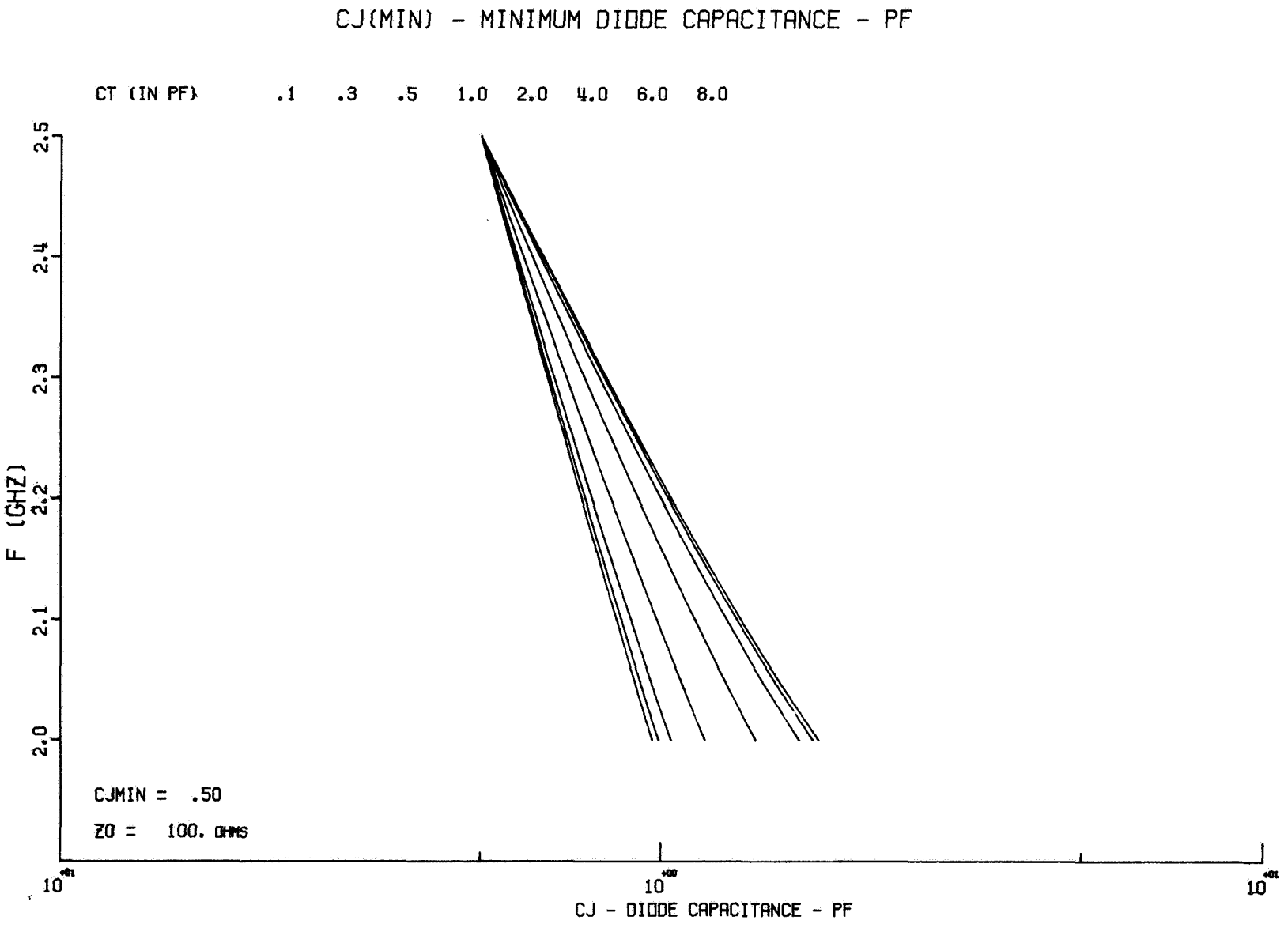

Figure 12. Tank Antiresonant Frequency Versus Diode Junction Capacitance with C_T as a Parameter

The tank circuit is now calculated using the Smith Chart for C_T equals 2.0 pF and C_{jmin} equals 0.46 pF as follows:

For C_j:

$$X_c = \frac{1}{6.28 \times 2.5 \times 10^9 \times 0.46 \times 10^{-12}}$$

$$= \frac{1}{7.23 \times 10^{-3}}$$

$$= 0.1385 \times 10^3$$

X_c = 138.5Ω plotted as capacitance in Figure 13

For C_T:

$$X_c = \frac{1}{6.28 \times 2.5 \times 10^9 \times 2 \times 10^{-12}}$$

$$= \frac{1}{31.4 \times 10^{-3}}$$

X_c = 31.8Ω plotted as inductance in Figure 13

From Figure 13 the total length would be

$$l_t = \lambda_T + \lambda_j$$

$$= 0.0485 + 0.15$$

$$l_t = 0.1985\ \lambda$$

At 2.5 GHz a wavelength is

$$\lambda = \frac{300}{2.5 \times 10^3 \times 1.38}$$

$$= 8.7 \text{ cm}$$

λ = 3.42 inches

and the total length would be

l_t = 1.725 cm

l_t = 680 mils

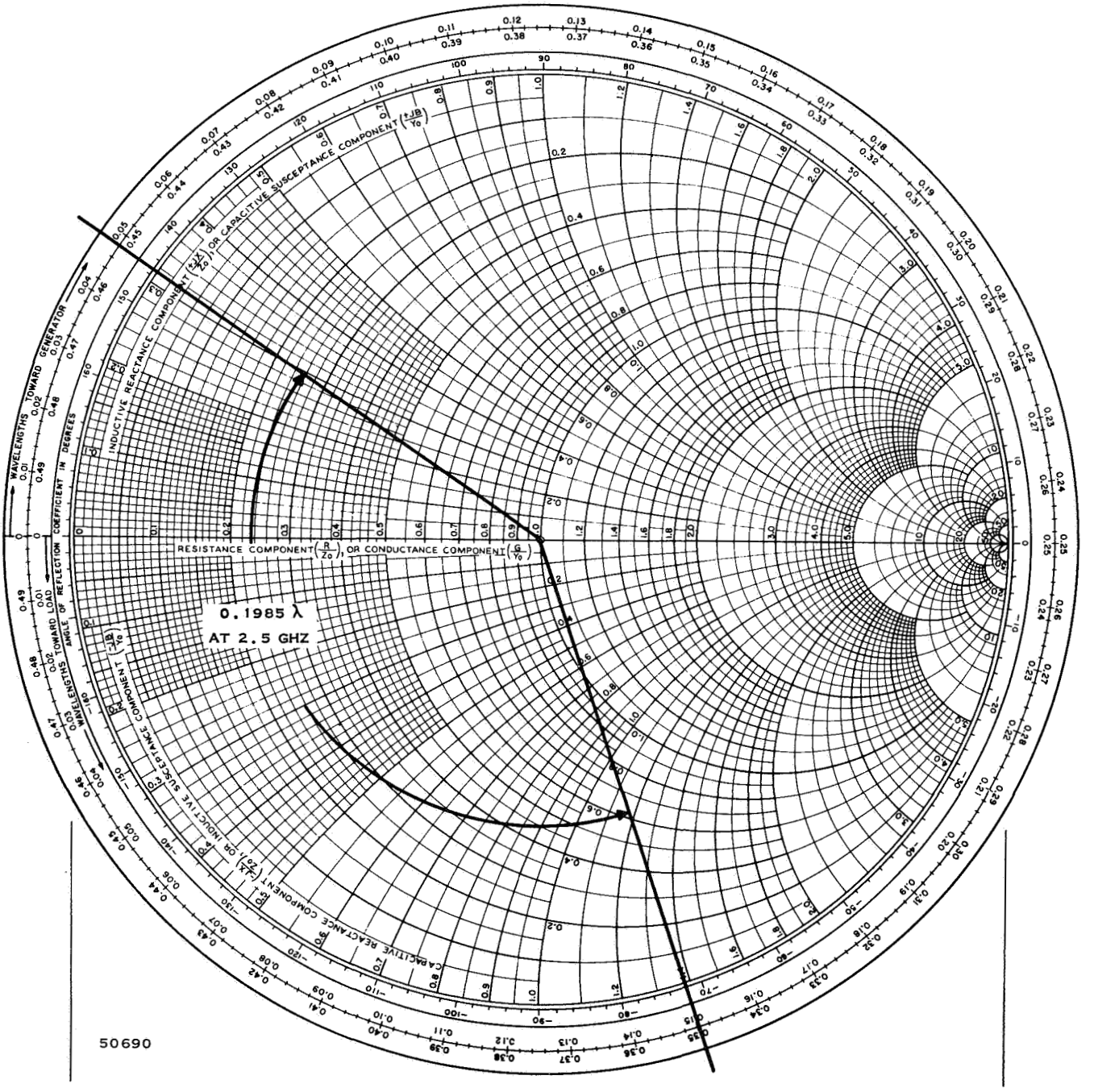

Figure 13. Tank Circuit Calculations

The quarter wavelength emitter and collector lines will be made for the average frequency, 2.25 GHz

$$\lambda = \frac{300}{2.25 \times 10^3 \times 1.38}$$

$$= 9.67 \text{ cm}$$

$$= 3810 \text{ mils}$$

Therefore

$$\frac{\lambda}{4} = 952.5 \text{ mils}$$

The new design produced results that were lower than expected in frequency and power. Figure 14 shows power output versus frequency for the design. The varactor voltage required to tune the desired range could not be located, as the maximum frequency was approximately 2080 MHz. In an effort to define the frequency range, a half-wavelength ($\lambda/2$) line was added to the emitter tab. This gives the capability of cutting the emitter tab to raise the frequency, while leaving the original tab intact.

By cutting the emitter tab, the oscillator frequency was raised to the desired band and the output power could be detected. Table II shows how the length of line affected the tank circuit.

Table II. Effects of Emitter Tab

l_E (inches)	P_O (mW)	Freq. (MHz)	V_D (volts)	Voltage Tap (mils)	Output Tap (mils)
2.398	37	2163	3.8	205	30 (from end of line)
2.371	36	2180	4.1		
2.351	35	2197	4.6		
2.332	34	2208	4.8		
2.310	34	2227	5.1		

After determining the best length for the emitter tab, data were taken which showed that a varactor voltage of 3 to 23.7 volts was required to tune 100 MHz. Figure 15 shows the power output versus frequency for this configuration. The data also showed that the emitter current had to be at least 42 mA or oscillation would not occur. The data taken clearly show that both the tank circuit and starting conditions are not optimum.

In an effort to achieve the optimum design the transistor parameters must be obtained for the desired band of operation. In order to achieve this, devices were put into packages and the input and output parameters calculated.

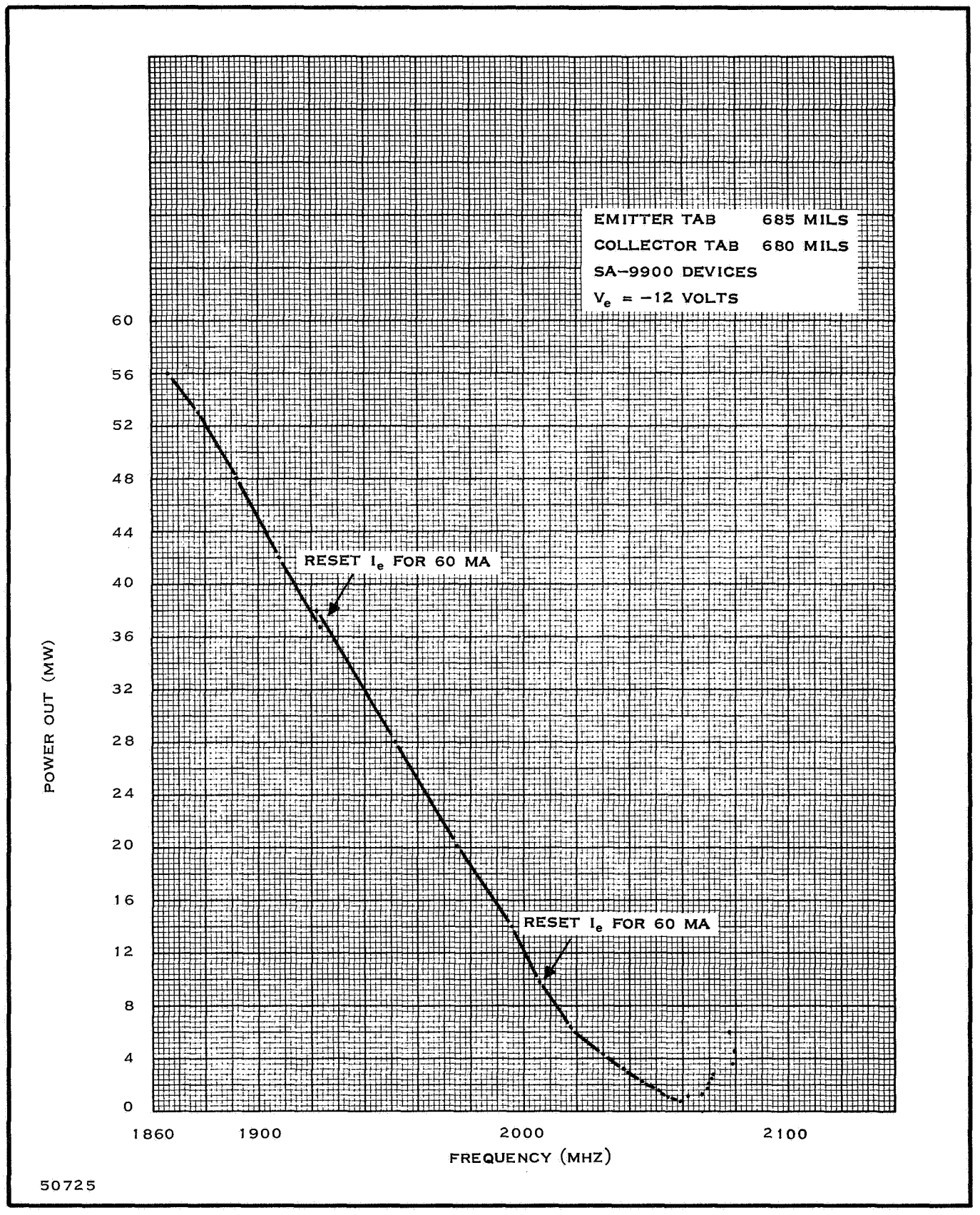

Figure 14. Power Output Versus Frequency

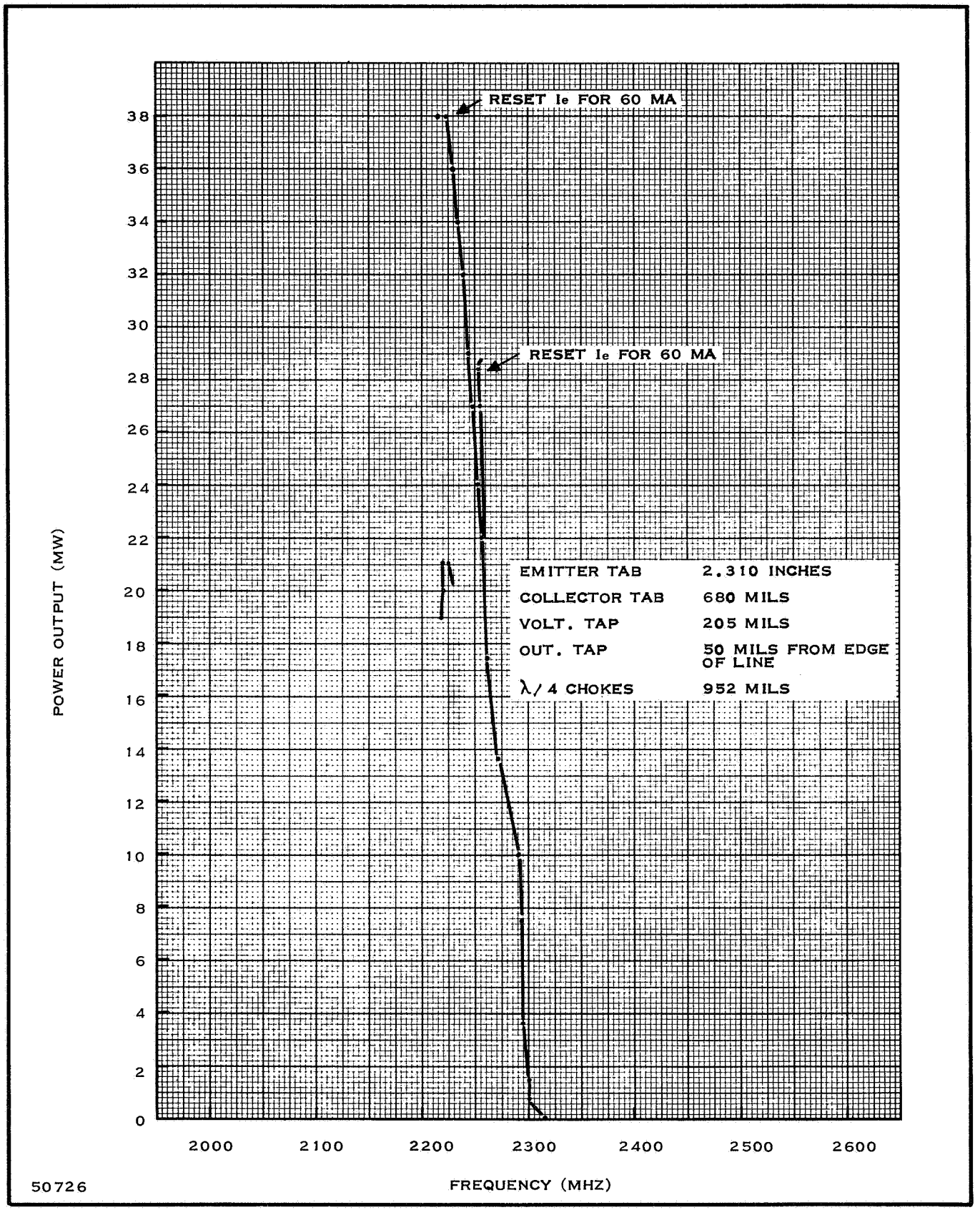

Figure 15. Power Output Versus Frequency

The test setup is the same as the one used for device characterization (Figure 16). The device is removed from the test setup after maximum power transfer is achieved, and a slotted line is used to measure the input and output VSWR and minimum points.

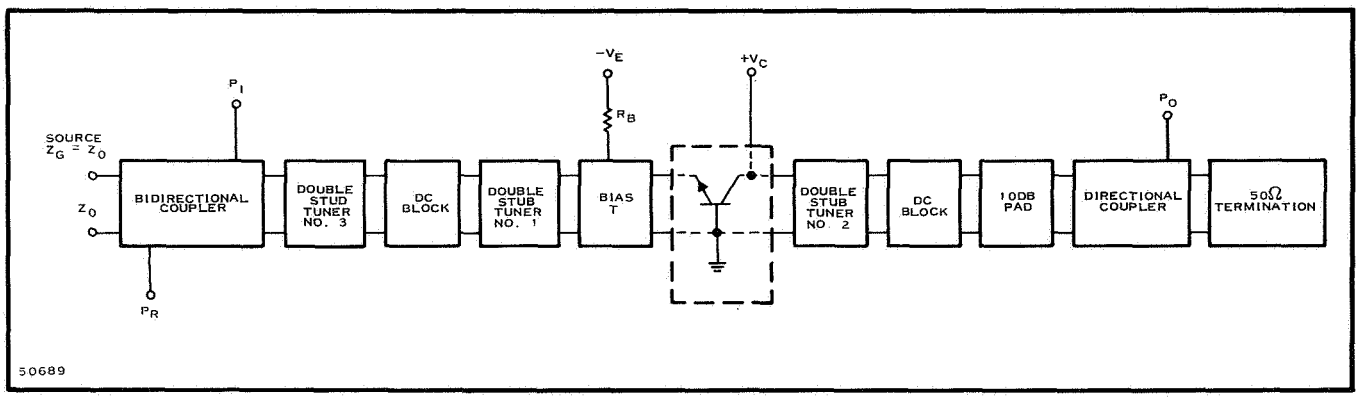

Figure 16. Class A Characterization Test Circuit Block Diagram

As an example at 2.25 GHz the following data were obtained:

VSWR		MINIMUM		GEN (0)	LOAD (450)
Input	Output	Input	Output	Minimum	Minimum
3.85	3.95	213.1	240.6	194.6	261.2

The fraction of the wavelength to be rotated toward the generator is given by:

$$\Delta\lambda = \frac{\text{Inp. Min - Gen. min.}}{2(\text{load min. - Gen. min.})}$$

$$\Delta\lambda = \frac{213.1 - 194.6}{2(261.2 - 194.6)}$$

$$\Delta\lambda = 0.1388 \quad \text{toward generator}$$

and the fraction of wavelength toward the load (replace input by output) is:

$$\Delta'\lambda = \frac{261.2 - 240.6}{2(261.2 - 194.6)}$$

$$\Delta'\lambda = 0.1546\ \lambda \text{ toward the load}$$

Rotating these amounts would yield the admittances at the package terminals, therefore the addition of the package must be accounted for to find the

chip parameters. To find the chip admittances the package admittances are rotated through 4.5 mm (collector) and 5.5 mm (emitter). This yields a fractional wavelength of

$$\Delta\lambda = \frac{4.5}{133.2} = 0.0338\lambda$$

$$\Delta\lambda = \frac{5.5}{133.2} = 0.0413\lambda$$

Therefore, the total wavelength for a given frequency would be the sum of the following distances:

1. Chip to TI-line* package
2. TI-line package to Tellite fixture
3. Tellite fixture to stubs

or 0.2651 λ toward generator and 0.5234 λ toward the load. These points are shown in Figure 17, and yield the following normalized input and output admittances, respectively: 3.4 - j 1.1 and o.26 - j o.15. For 20×10^{-3} mho the input admittance is 68 - j 22 millimhos, while the output admittance is 5.2 - j 3.0 millimhos. Therefore the output capacitance would be:

$$C_T = \frac{1}{2\pi f x_c}$$

where

$$X_C = \frac{1}{jB}$$

$$= \frac{1}{3 \times 10^{-3}}$$

$$X_c = 333 \text{ ohms}$$

and

$$C_T = \frac{1}{6.28 \times 2.25 \times 10^9 \times 3.33 \times 10^2}$$

$$= \frac{1}{47 \times 10^{11}}$$

$$= 0.0213 \times 10^{-11}$$

$$C_T = 0.213 \text{ pF}$$

This value of C_T does not agree with the data sheets. According to data taken, the average maximum capacitance is 1.7 pF for 0.1 volt from collector to base. In the actual circuit V_{CB} is 12 volts and C_{ob} is 1.0 pF for a packaged device (chip 0.6 pF). This means that the output frequency should increase instead of decrease. These data indicate that the circuit parameters are not optimized.

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* Registered Trademark of Texas Instruments, Incorporated

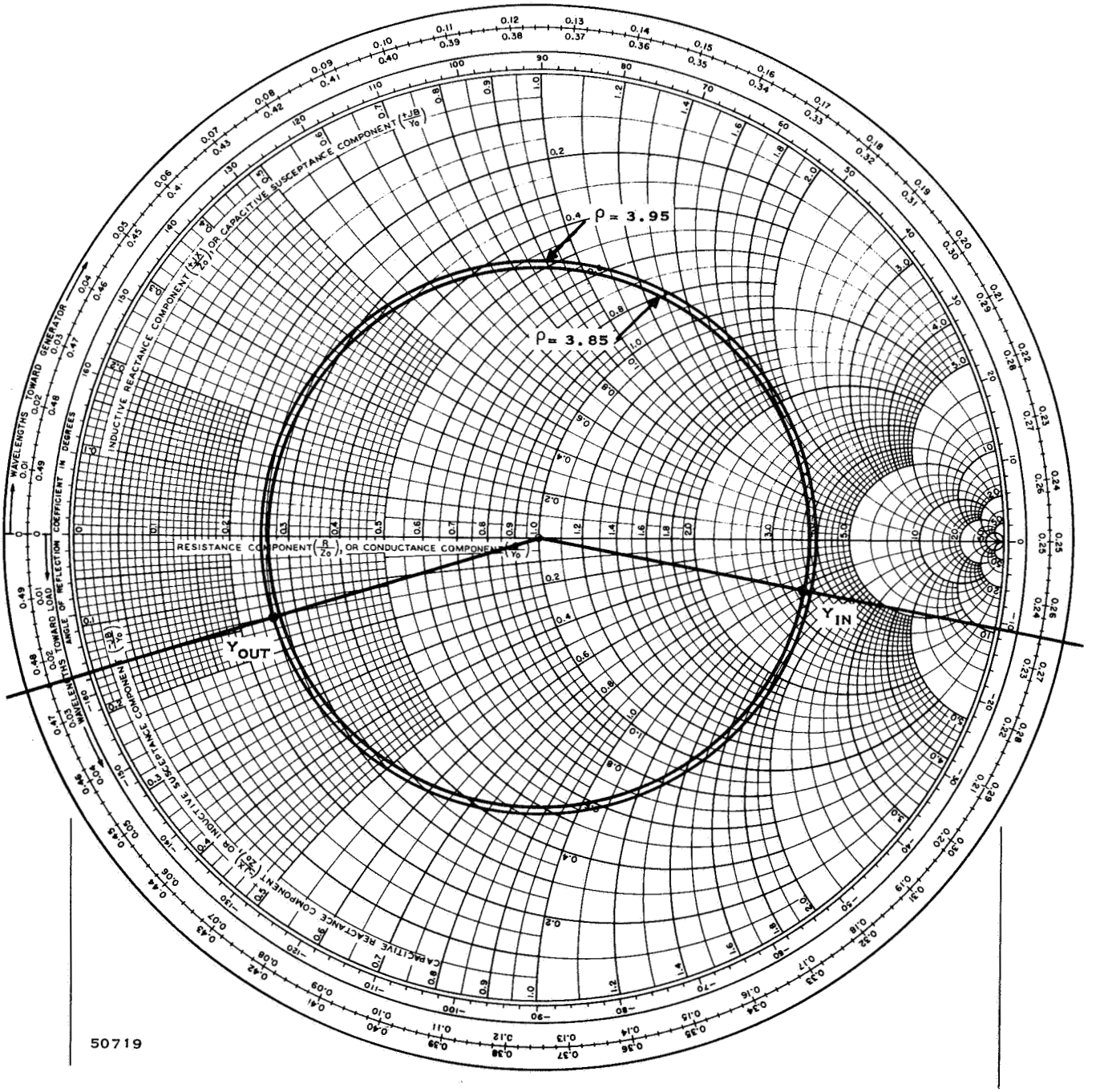


Figure 17. Normalized Input and Output Admittances

In an effort to determine why the required frequency and power output could not be obtained in any of the circuits the relationship between diode cutoff frequency and tank insertion loss was evaluated. The unloaded [5]Q of the tank is

$$Q_u = \frac{1}{G_D \times C_T} \tag{9}$$

The loaded Q of the tank is

$$Q_L = \frac{1}{(G_D + G_p + G_L) X_{CT}} \tag{10}$$

Now

$$R_s = \frac{159}{f_{co} C_s} \tag{11}$$

where

R_p = effective parallel real part of the transistor output impedance

R_L = transformed load, real part

R_D = total parallel real part of the tank circuit and is considered to be due to the diode

R_s = series resistance of the diode

C_s = series capacitance of the diode, in pF

f_{co} = diode cutoff frequency, in GHz

C_T = total tank shunt capacitance

The diode Q is given by

$$Q_u = \frac{f_{co}}{f_o} \tag{12}$$

which is essentially the unloaded Q of the tank since the transmission line can be considered lossless

$$R_D = R_s (1 + Q^2) \tag{13}$$

substituting equation (11) into (13) for R_S and then (12) into (13) and inverting yields

$$G_D = \frac{f_{co} C_S}{159 \left[1 + \left(\frac{f_{co}}{f_o}\right)^2\right]} \qquad (14)$$

$$= \frac{C_S}{159\left[\frac{1}{f_{co}} + \frac{f_{co}}{(f_o)^2}\right]}$$

To determine G_D the following data were used:

C_s = 0.6 pF at 17V for 2.3 GHz

f_{co} = 50 GHz

which yielded

$$G_D = 4 \times 10^{-4}$$

Since the insertion loss is given by

$$\text{Loss} = 20 \log_{10} \frac{Q_u}{Q_u - Q_L} \qquad (15)$$

$$= 20 \log_{10} \frac{1}{1 - \frac{Q_L}{Q_u}}$$

The loaded to unloaded Q ratio is needed and is obtained from equations (9) and (10):

$$\frac{Q_L}{Q_u} = \frac{G_D}{G_D + G_p + G_L} \qquad (16)$$

Reasonable values for R_p and R_L would be 100 and 200 ohms, respectively, which yield

$$\frac{Q_L}{Q_u} = 3.58 \times 10^{-2}$$

Therefore the insertion loss would be

$$\text{Loss} = 20 \log_{10} \frac{1}{1 - 0.0358} \tag{16}$$

$$= 0.360 \text{ dB}$$

which is almost negligible.

Another area of investigation was the addition of inductance due to ball bond leads. In order to determine the effect of the leads their length was measured and the inductance calculated.[6]

$$L = 0.005\ell \left[2.3 \log_{10} \left(\frac{4\ell}{d} - 0.75\right)\right] \tag{17}$$

where

L = inductance in μH

ℓ = length of wire in inches

d = diameter of wire in inches

$$L = 0.005 \ (0.022) \left[2.3 \log_{10} \left(\frac{4(0.022)}{0.0007} - 0.75\right)\right]$$

$$L = 0.531 \text{ nH}$$

and

$$X_L = 7.5\Omega \text{ at } 2.25 \text{ GHz}$$

It can be said that if the ball bond leads are held as short as possible (preferably shorter than 15 mils) they should not cause any problems.

Since the varactor and ball bond leads seem to have caused very little degradation of the oscillator, some chip devices were packaged and tested in a standard stub tuner oscillator. This is the same tuner used to test the devices on the assembly line. Table III shows the data obtained on the five packaged devices.

The results of the tests showed that the devices fall off drastically at 2.2 GHz (1/3 of power) and probably are worse at 2.3 GHz. Therefore these devices will provide less power output than required from 2200 to 2300 MHz. For this reason these devices were abandoned and a new oscillator built.

TABLE III

Power Output for SA9900 Devices

Device	Voltage (V)	Current (mA)	Po (mW)	Frequency (GHz)
A	12	30	91	2.03
1	12	30	68.5	2.01
2	12	30	broken lead	
3	12	30	56	1.96
4	12	30	90	2.00
A	15	15	48.9	1.983
1	15	15	34.0	1.99
3	15	15	41.0	1.99
4	15	15	47.0	2.03
A	12	30	34.0	2.19
3	12	30	15.0	2.22

b. L-146-5B Device Oscillator

The new oscillator design was accomplished using a new device designed specifically for oscillator applications to 5 GHz. This device (Figure 18) was characterized using s-parameter data and the results were used in the VCO design.

The design procedure employed a computer program for converting s parameters to h and y parameters. Two programs[7] written at Texas Instruments for the IBM 7040 calculate the y, h, and s parameters, stability quality, maximum stable gain, unilateral gain, and maximum available gain of transistors.

The first program, called the equivalent circuit program, takes the transistor equivalent circuits described and, given a set of element values, computes the parameters for the three transistor configurations. The second program, called the parameter conversion program, accepts a set of measured y, h, or s parameters as input and computes the remainder of the parameters. The parameter conversion program also has the facility for mathematically removing the effect of a given set of header parasitics and/or replacing them with another set. Thus, knowing the two port parameters of a transistor chip in a given header, we can obtain the performance and two-port parameters of the chip either by itself or in another type of header.

Without access to programs such as these, correlations between measured parameters and an equivalent circuit would involve very tedious hand calculations; therefore, it would be necessary to use rather crude approximations which usually neglect header parasitics.

The measured data for the L-146-5B device are shown in Table IV.

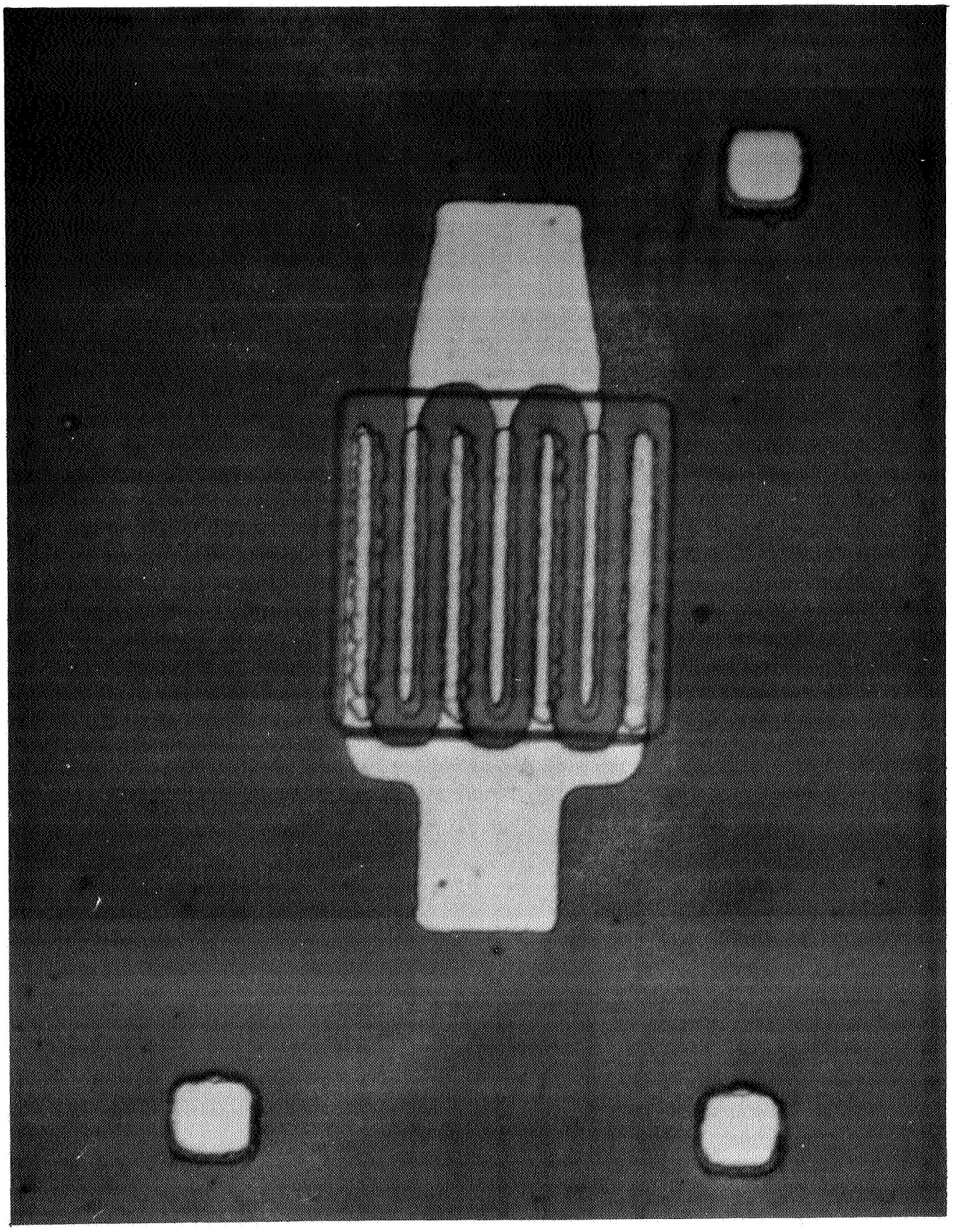


Figure 18. L-146 Geometry

TABLE IV

s Parameter Data

s_{11}	= 0.654 $\angle$ 185	
s_{12}	= 1.52 $\angle$ 72.1°	Data at 2.5 GHz
s_{21}	= 0.0717 $\angle$ 69.7°	in common emitter con-
s_{22}	= 0.516 $\angle$ 313°	figuration

The computer then transformed these data into h and y parameters to be used in the design of the oscillator. The program yielded the following chip parameters:

$$h_{11} = 13.1 - j3.69 \qquad y_{11} = (7.08 + j2)\ 10^{-2}$$

$$h_{12} = (9.21 + j63.9)\ 10^{-3} \qquad y_{12} = (.625 - j4.71)\ 10^{-3}$$

$$h_{21} = -1.36 \times 10^{-1} - j1.36 \qquad y_{21} = (1.75 - j9.89)\ 10^{-2}$$

$$h_{22} = (8.81 + j7.34)\ 10^{-3} \qquad y_{22} = (2.33 + j7.14)\ 10^{-3}$$

From the above data the starting conditions can be determined when h_{fb} and the emitter-to-collector capacitance are known.

$$h_{fb} = \frac{h_{11}}{1 + h_{11}}$$

$$h_{fb} = -0.845 \ \angle 321.8°$$

The emitter-to-collector capacitance is obtained from

$$y_{22} = (2.33 + j7.14) \times 10^{-3}$$

where C_{ec} would be

$$C_{ec} = \frac{1}{2\pi f x_c}$$

and

$$X_c = \frac{1}{jB}$$

$$= 140\ \Omega$$

$$C_{ec} = 0.45\ pF$$

The value of the emitter capacitance can now be calculated by

$$h_{fb} > \frac{C_2}{C_1 + C_2}$$

where C_1 and C_2 are defined as the emitter-to-base and emitter-to-collector capacitance respectively.

$$\therefore C_1 = 0.14 \text{ pF}$$

For the inequality to be satisfied, C_1 must be greater than 0.14 pF. The optimum value is usually 2 to 4 times this value; a value of 0.35 pF is assumed.

The length of the emitter tab would be

$$l = VZC$$

$$= \frac{3 \times 10^{10}}{1.38} \times 40 \times 3.5 \times 10^{-13}$$

$$= 120 \text{ mils}$$

The tank circuit analysis is made by assuming a terminating capacitor and investigating the tank and diode constants required to obtain a given tuning range.

Using the data obtained, the output capacitance for two devices in parallel would be

$$C_t = C_{ob} + C_{FB}$$

$$= 2(0.4) + \frac{0.35(0.45)}{0.35 + 0.45}$$

$$C_t = 0.99 \text{ pF}$$

The Smith Chart is now used to calculate the tank circuit.

For C_t:

$$X_{C_T} = \frac{1}{6.28 \times 2.5 \times 10^{9} \times 10^{-12}}$$

$$= 63.7 \ \Omega$$

For C_j:

$$X_{C_j} = \frac{1}{6.28 \times 2.5 \times 10^{9} \times .4 \times 10^{-12}}$$

$$= 159 \ \Omega$$

Therefore the total length of line would be (Figure 19)

$$l_t = \lambda_{ct} + \lambda_{cj}$$

$$l_t = 0.25$$

$$l_t = 855 \text{ mils}$$

From the computer print out for C_{jmin} equals 0.4 pF the capacitance required for 2.2 and 2.3 GHz will be 0.77 pF and 0.62 pF respectively, which corresponds to a voltage of 6 and 9.8 volts.

The VCO was breadboarded as shown in Figure 20 and the results obtained after optimizing the location of the output tap and the length of the emitter tab are shown in Figure 21.

The power output at 2.2GHz is 34 mW and at 2.3 GHz is 40 mW for varactor voltages of 9 and 18 volts, respectively. The total loss within the band is 0.8 dB.

Temperature tests were conducted over a temperature range of -28°C to +71°C with the results shown in Table V.

TABLE V

Temperature Tests

Temperature	Frequency	Po
°C	MHz	mW
71	2244.8	21.5
65	2244.9	22.5
55	2246.4	25
45	2247.6	27
35	2249.1	30
25	2250.5	32
16	2255.0	32
5	2256.3	34
-5	2258.2	37
-15	2260.2	39
-28	2263.0	42

The tests were conducted using a supply voltage of 15 volts, an initial varactor bias of 10.9 volts (2250 MHz) and an emitter current of 25 ma. The total frequency change of 18.2 MHz is within the specification limits of ±0.5% (±11.5 MHz).

In order to evaluate the reproducibility of the circuit, a second breadboard was constructed using newer devices.

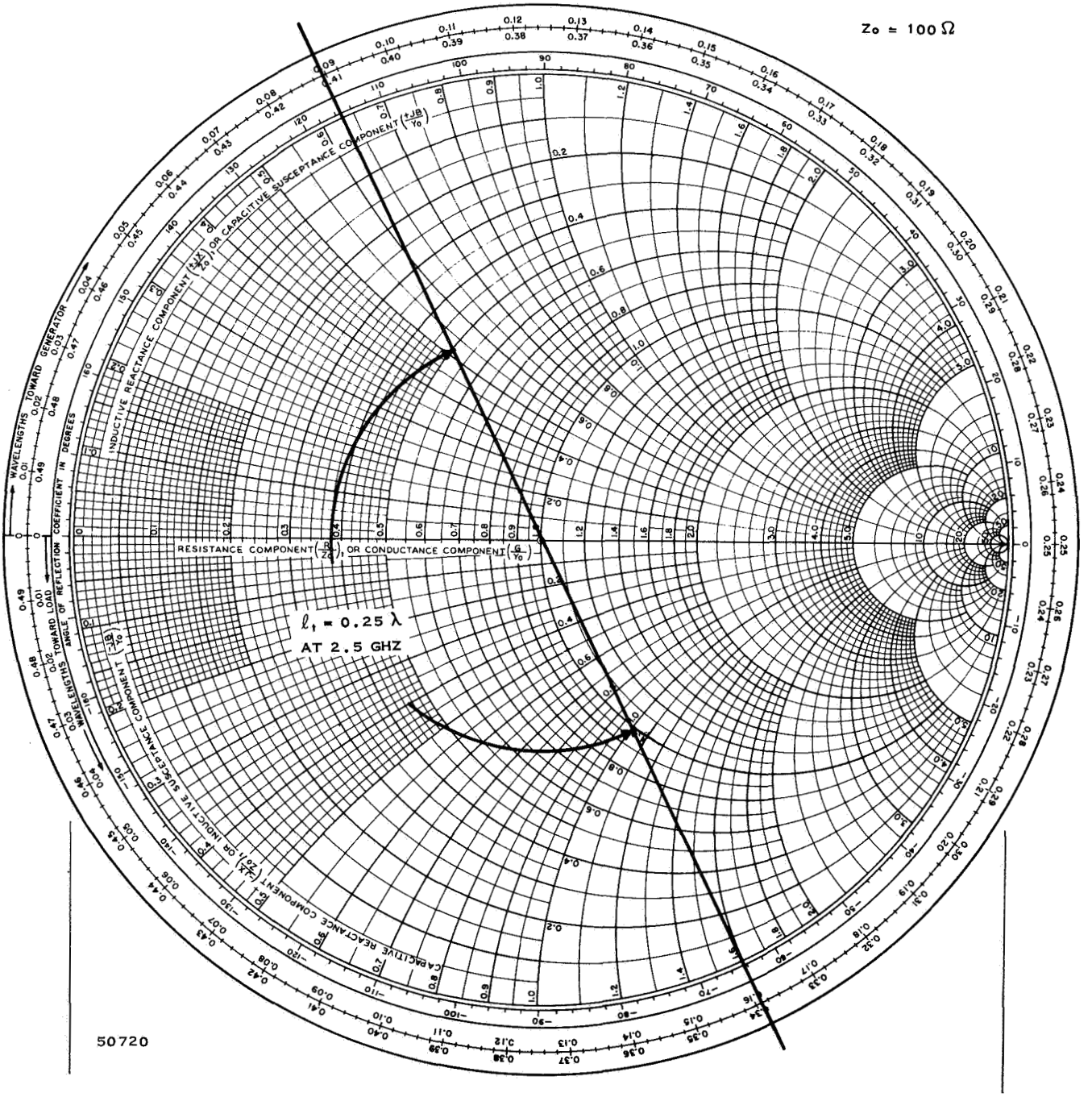


Figure 19. Tank Circuit Calculations

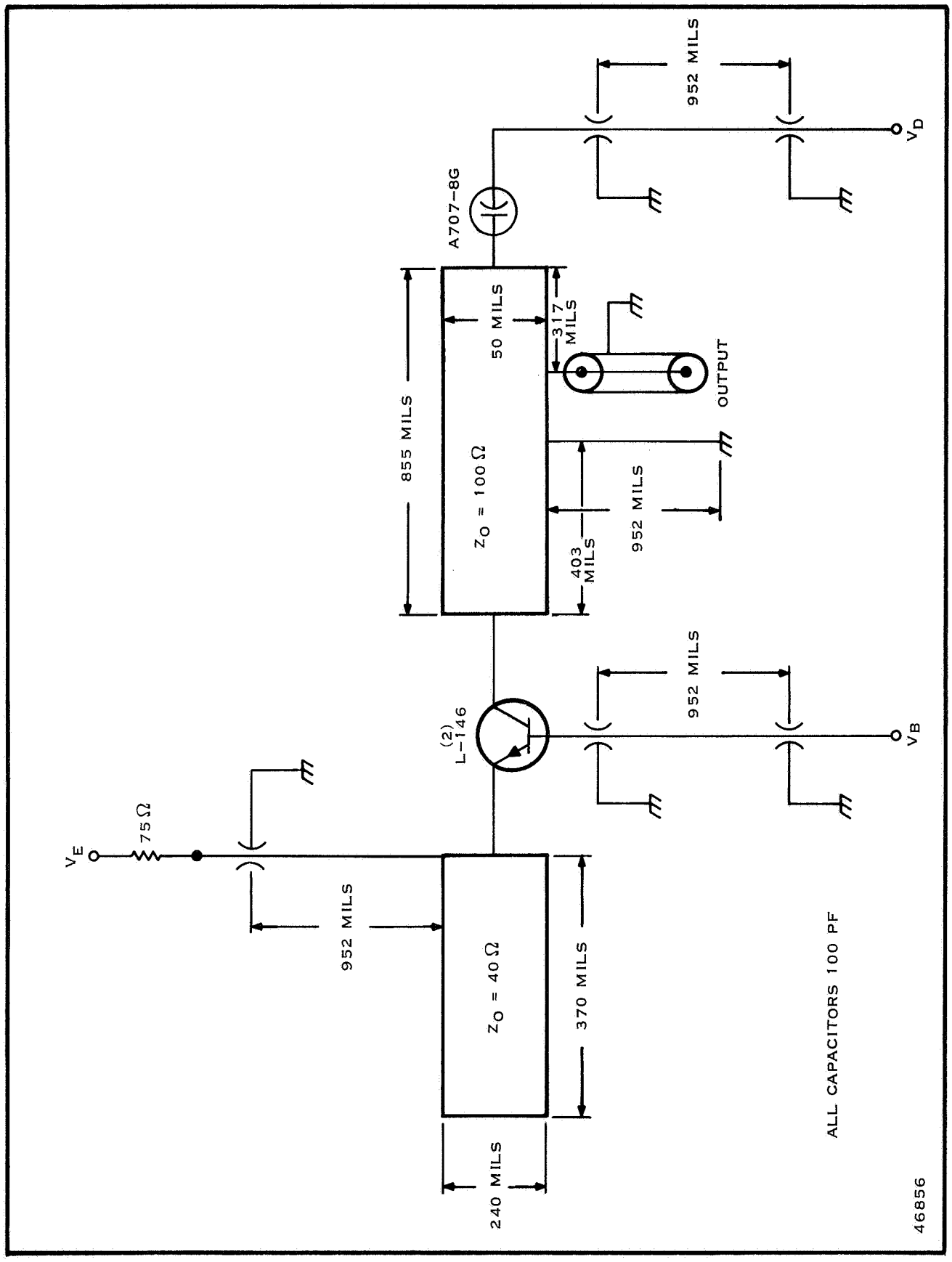


Figure 20. Breadboard VCO Layout

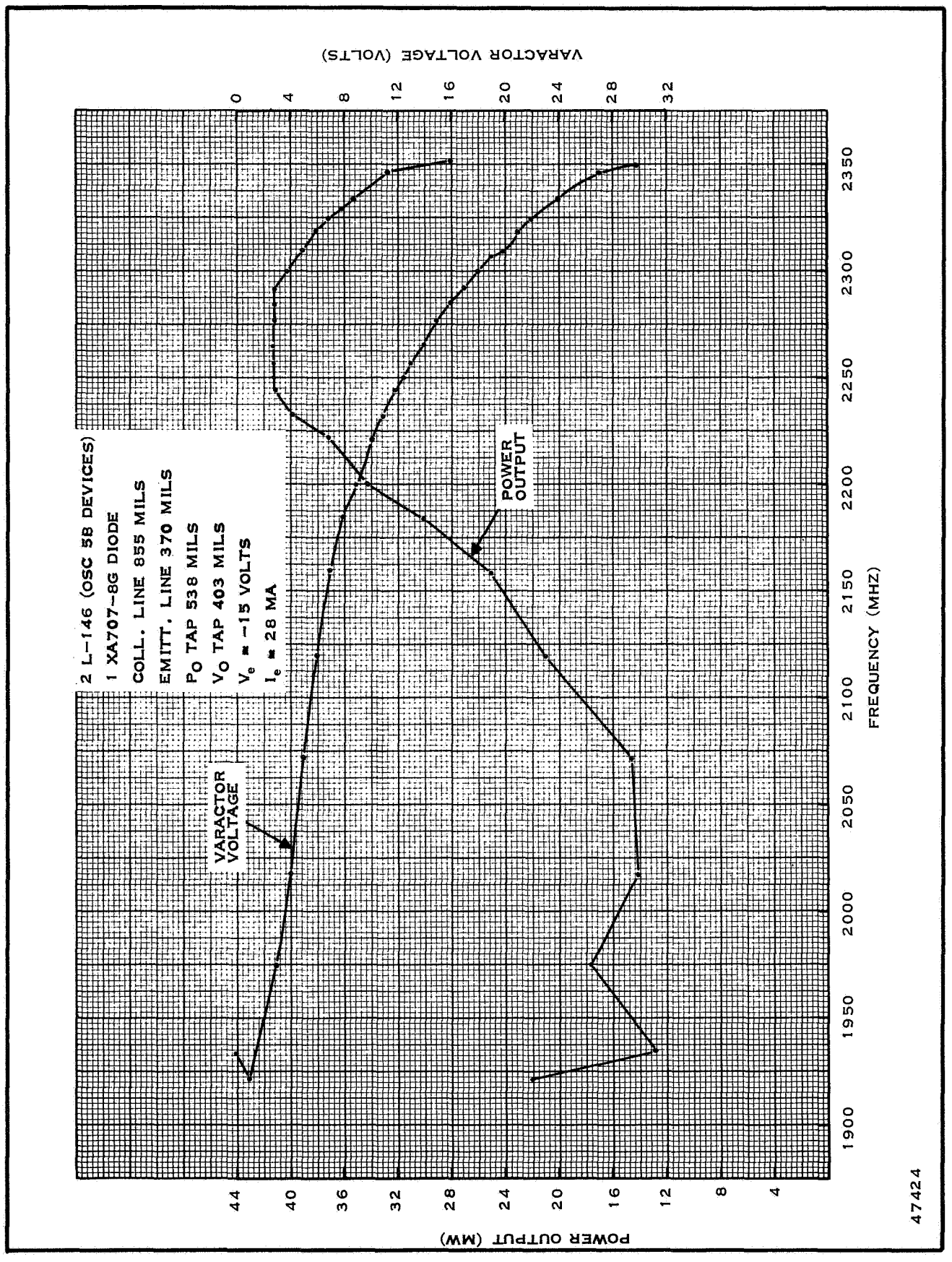


Figure 21. Breadboard VCO Performance

c. L-146-6C Device Oscillator

The new oscillator was fabricated with L-146-6C devices in the same circuit configuation as the L-146-5B oscillator (Figure 20). The output power of this model was over 100 mW and a much higher varactor voltage was required to tune the desired range. This indicated that the initial breadboard was faulty. This fact was confirmed by microscopic examination which revealed that several of the emitter fingers on one of the devices were open.

The circuit was revised slightly to compensate for the device parameter variations and an output above 100mW was obtained. Figure 22 shows the output power for the oscillator, which is 117 mW at 2200 MHz and 142 mW at 2300 MHz for a variation of 0.83dB. The varactor voltages required were 8.9 and 14 volts, respectively.

In order to realize a ceramic chip that would be as small as possible, two quarter-wavelength lines were removed. The final circuit layout is shown in Figure 23. This circuit presently is being converted to ceramic.

3. Ceramic Design

The ceramic layout was started employing chip ceramic capacitors to reduce fabrication time. As the transition to the ceramic substrate is accomplished, the chip capacitors will be replaced by thin-film types.

The actual circuit layout is shown in Figure 24 and measures 300 mils by 320 mils. It is anticipated that when the final oscillator is built the modulator will appear on the same substrate.

4. Modulator

The purpose of the modulator is to provide the desired modulation input impedance of 600 ohms, improve deviation linearity, establish modulation frequency response characteristics, isolate the modulation source from the VCO tank circuit, and establish the desired deviation sensitivity of 0.2 VRMS for 100 kHz deviation. Since a single-varactor VCO is being used, the modulation input will be at the same point as the error voltage.

It has been shown in the Third Scientific Report that the VCO sensitivity is 3.2 volts per 100 MHz deviation, or 0.00226 VRMS per 100 kHz. This indicates that some form of attenuation will be required between the modulation source and the varactor and that the attenuation ratio will be approximately 0.0113.

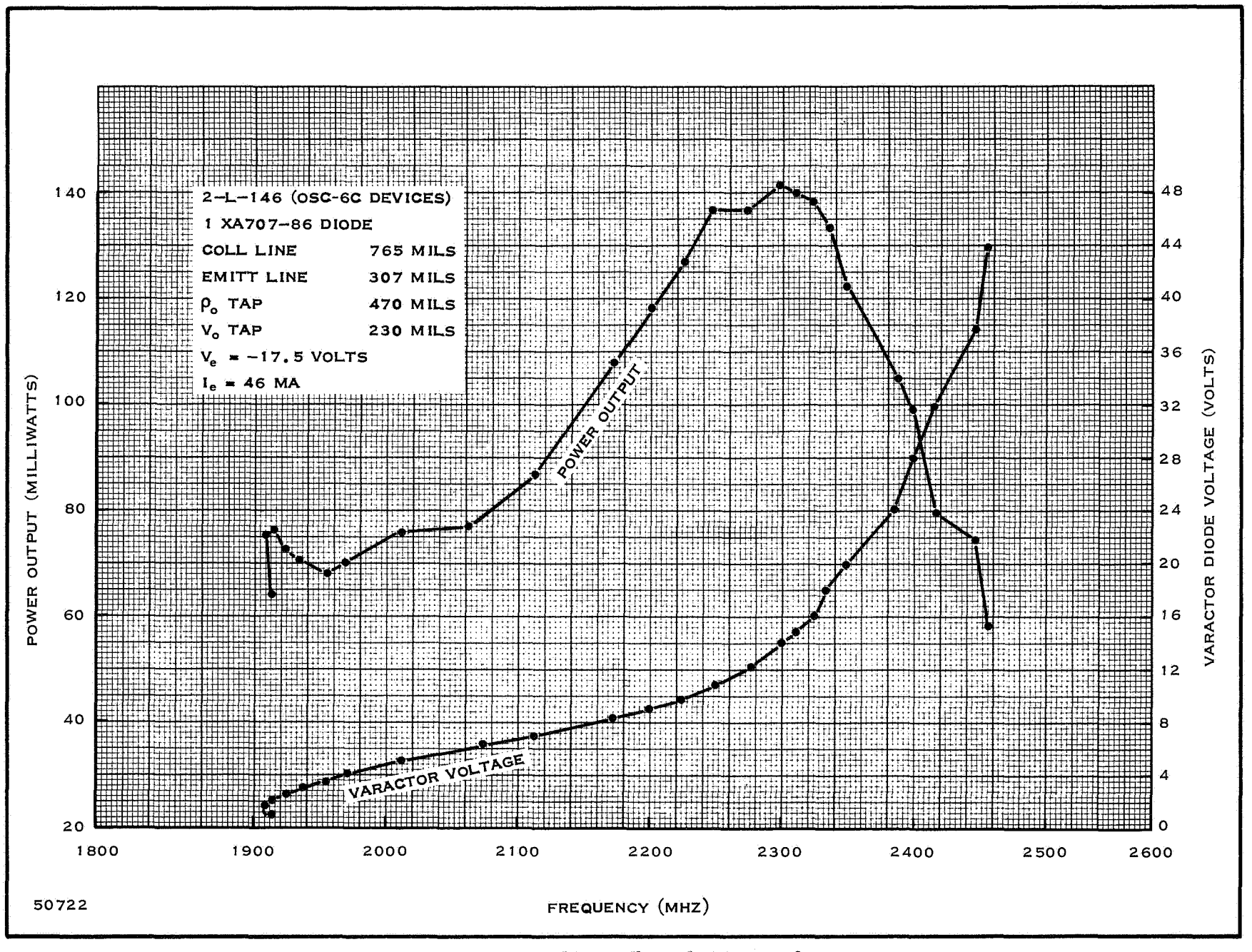


Figure 22. Revised Breadboard VCO Performance

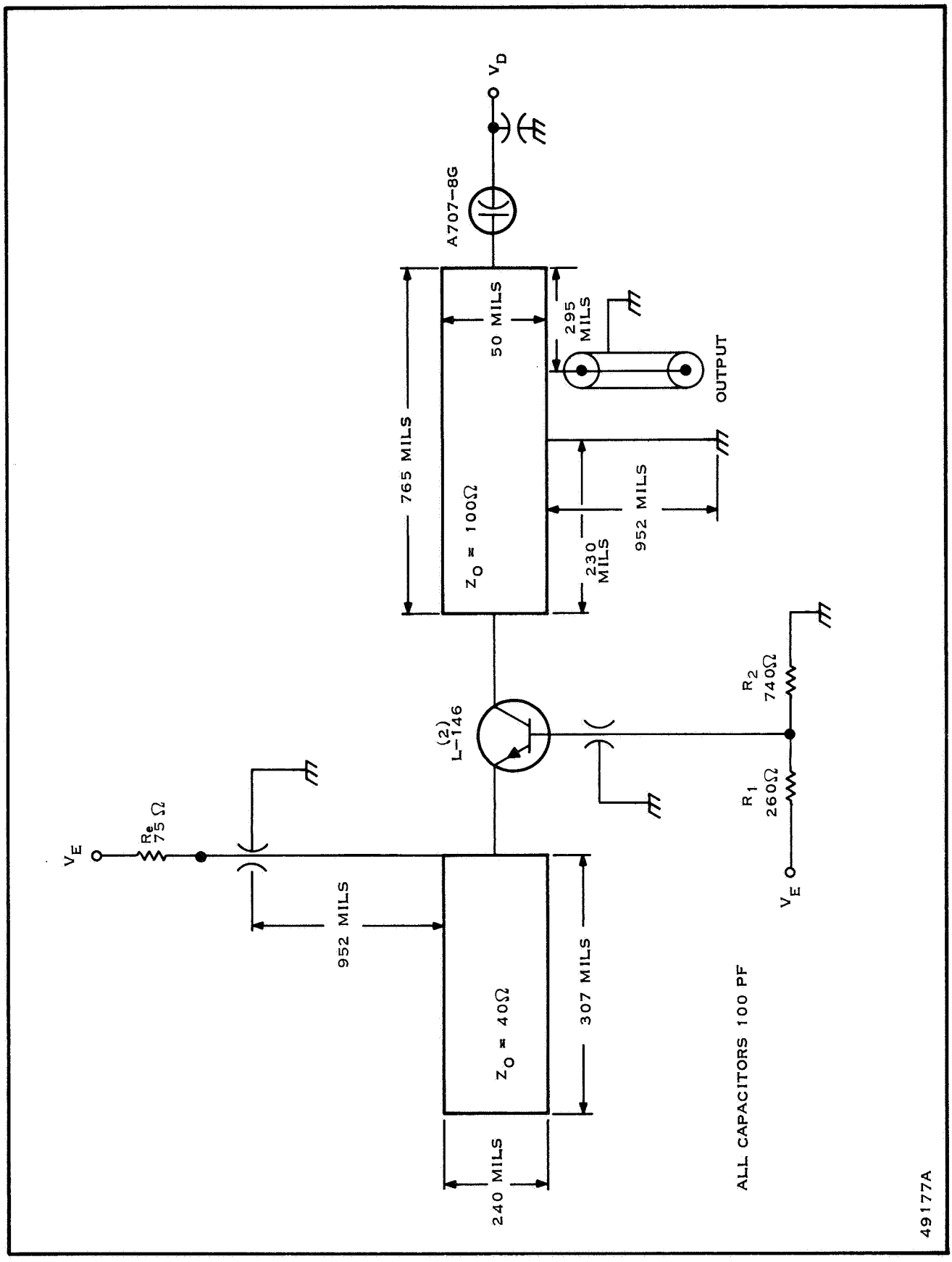


Figure 23. Revised Breadboard VCO Layout

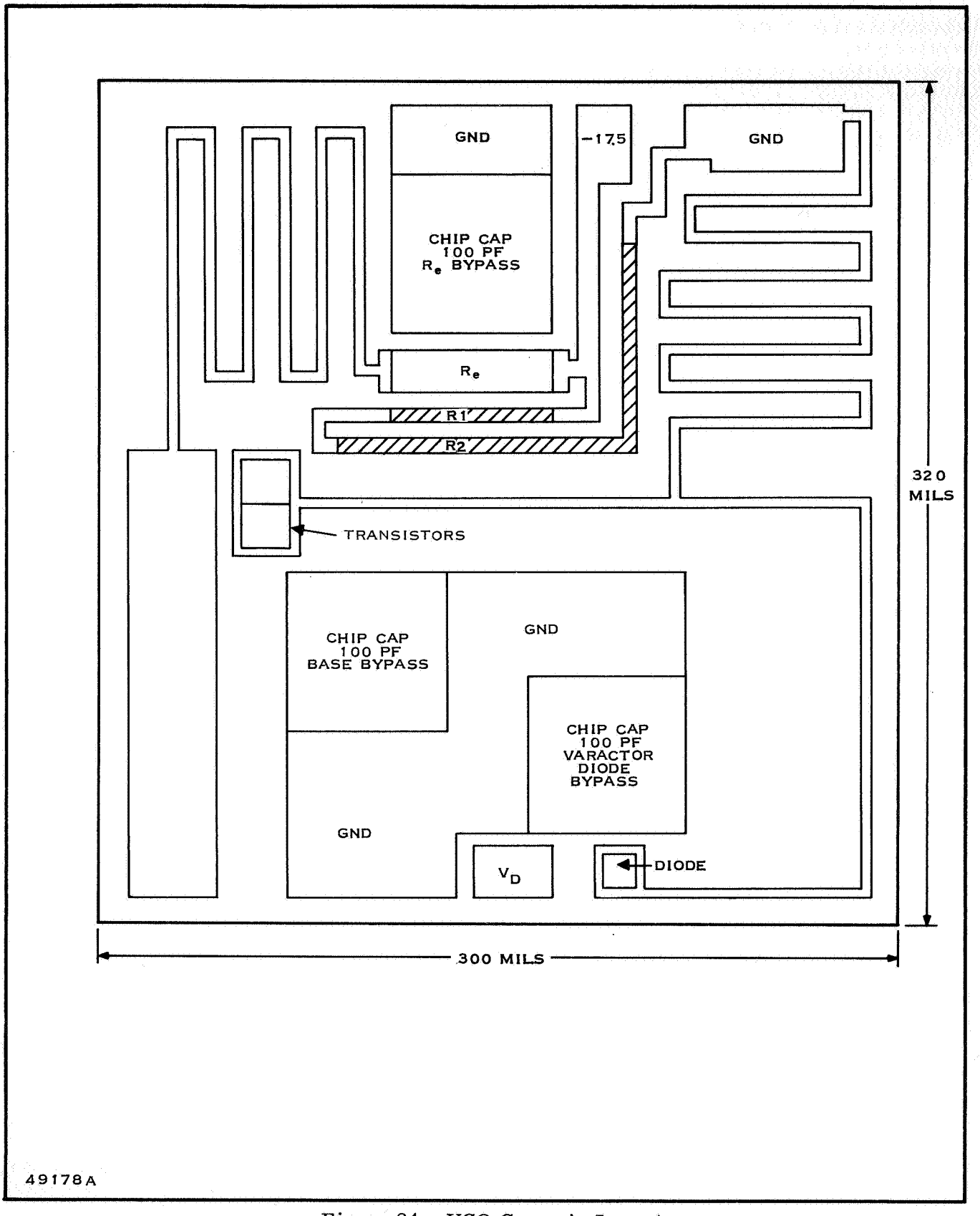


Figure 24. VCO Ceramic Layout

The original modulator design, Figure 25, was further investigated during the report period in an attempt to reduce the number of components required and to reduce the size of the capacitors employed to achieve the desired modulation response. In an attempt to flatten the frequency response, capacitance values became too large for thin-film techniques, and a new approach was sought.

The actual response was 0.98 VRMS to 0.0113 VRMS for 1 MHz and 2kHz, respectively, for a 1.0 volt RMS signal input, as shown in Figure 26.

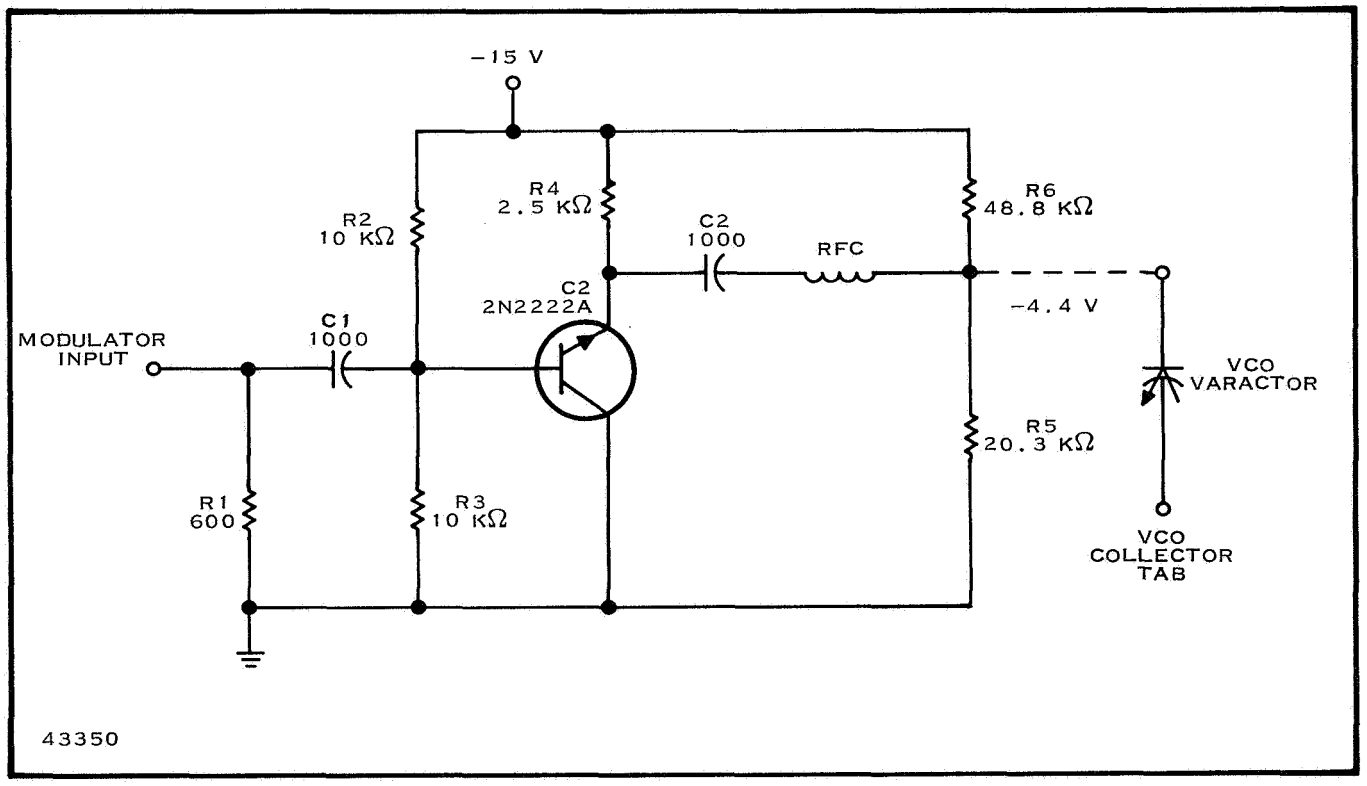


Figure 25. Modulator Schematic

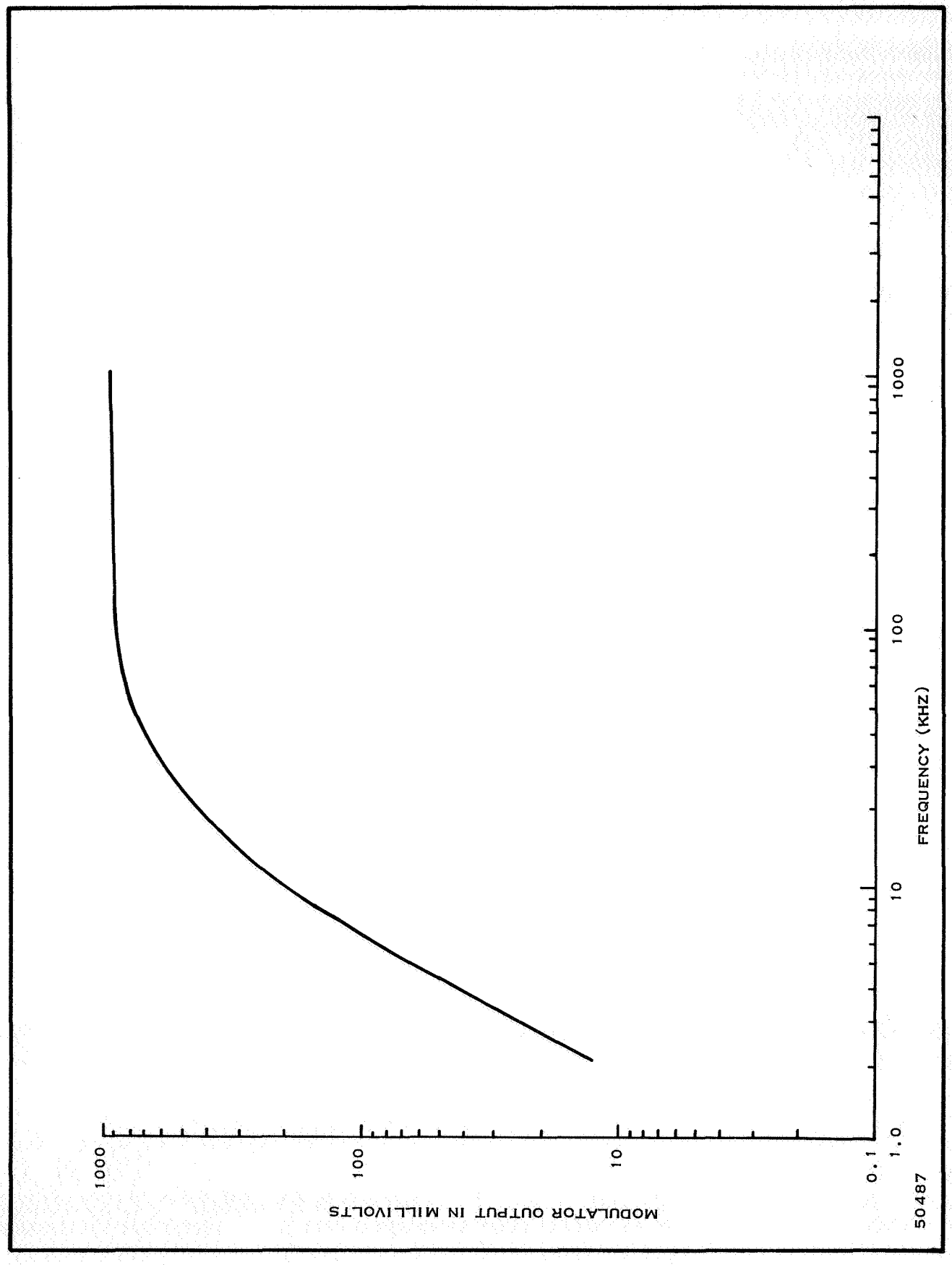


Figure 26. Modulator Response

The first alternate design approach employed an amplifier with feedback and the frequency response was improved. For a constant 1 VRMS input the output varied from 13.2 mV to 10.4 mV over the modulation frequency range. Figures 27 and 28 show the circuit layout and frequency response. This circuit required large capacitors and resistor values and was not considered suitable.

The second alternate design was entirely passive and contained only six elements: five resistors and one capacitor. For a constant 1.0 VRMS input the output of this circuit varied from 11.0 mV to 11.6 mV over the modulation frequency range. The circuit and frequency response are shown in Figures 29 and 30.

From the three designs tried, the passive modulator is best and will require the least area.

Since the final design of the oscillator was changed, the previously mentioned passive modulator will have to be redesigned.

The design of the final modulator is based on a deviation of 2.3 volts per 50 MHz or 0.00326 VRMS per 100 KHz. Therefore, the attenuation ratio required to meet a deviation of 0.2 VRMS per 100 KHz would be 0.0163.

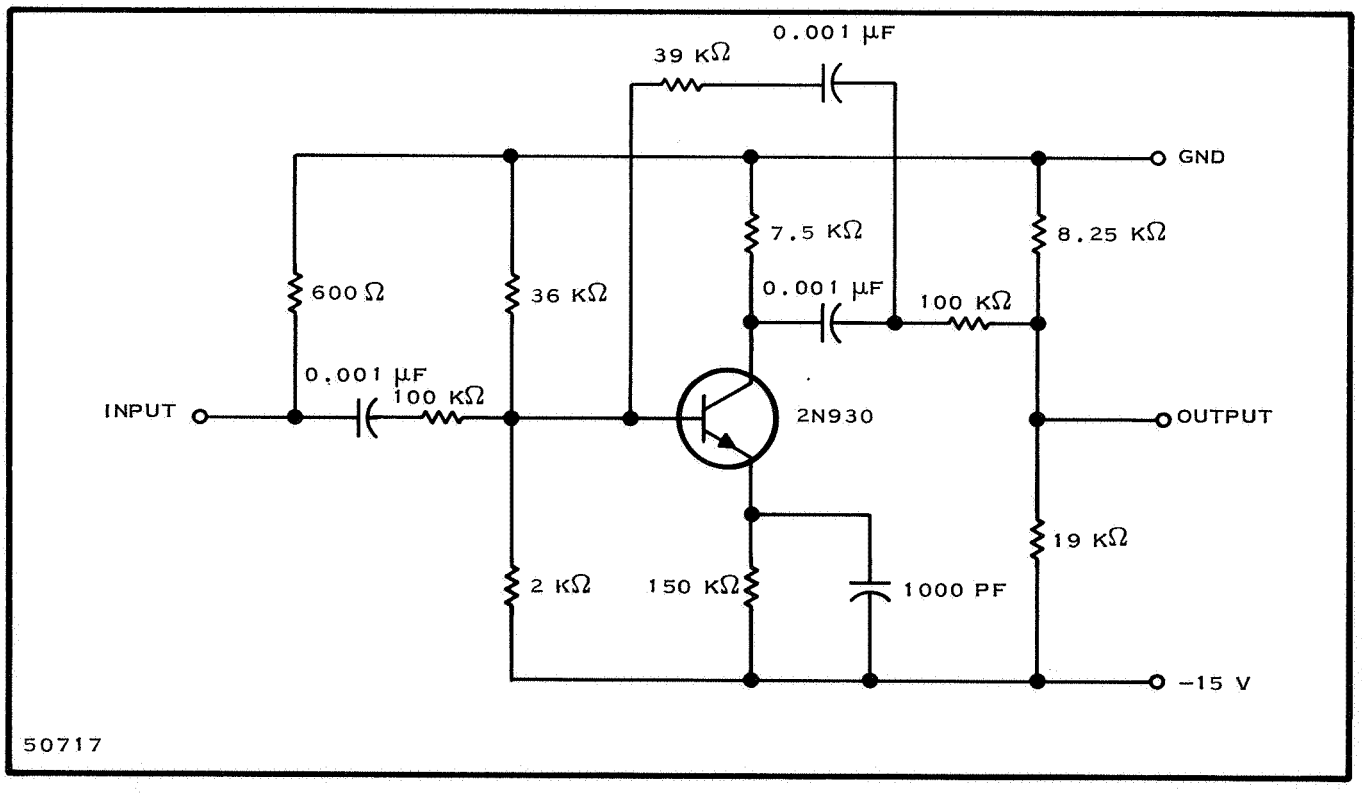


Figure 27. Active Modulator Schematic

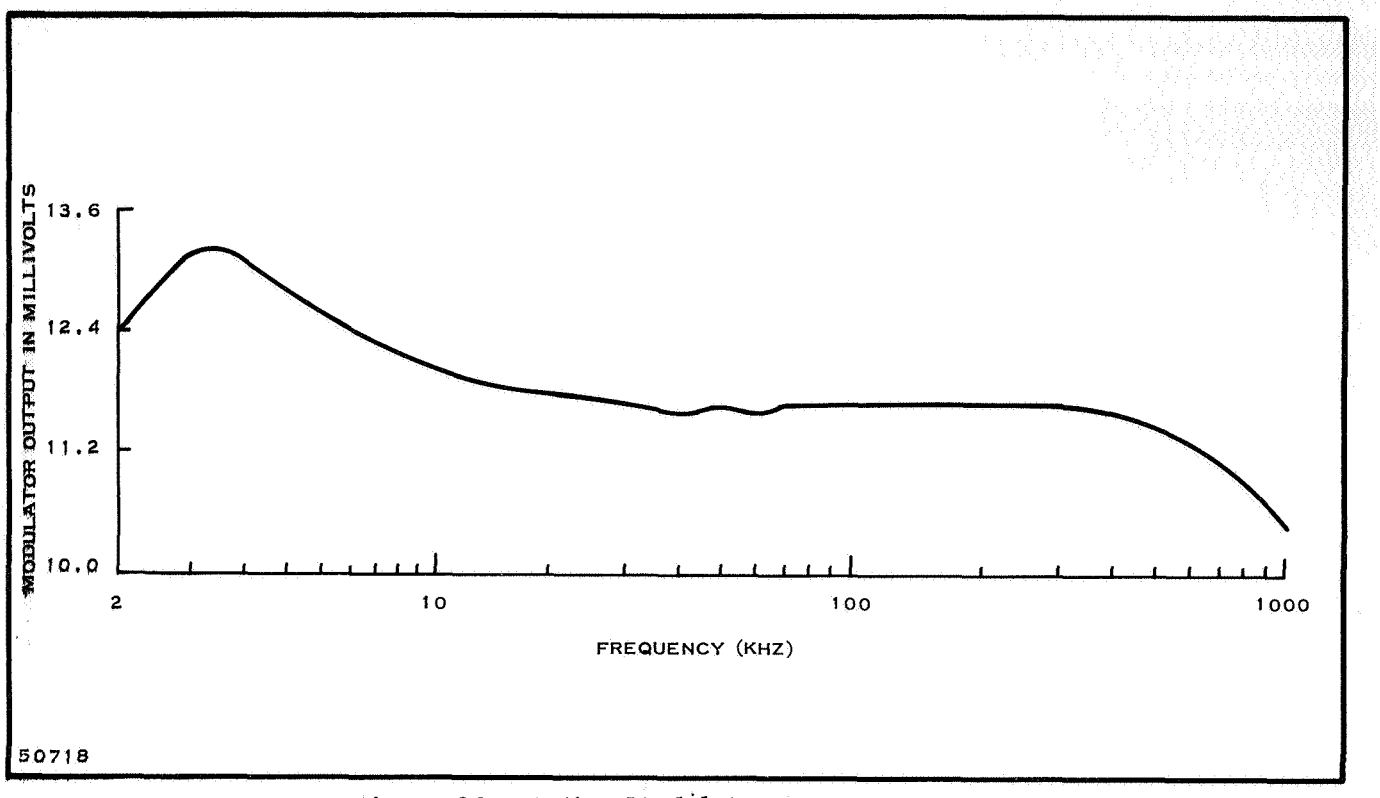


Figure 28. Active Modulator Output Response

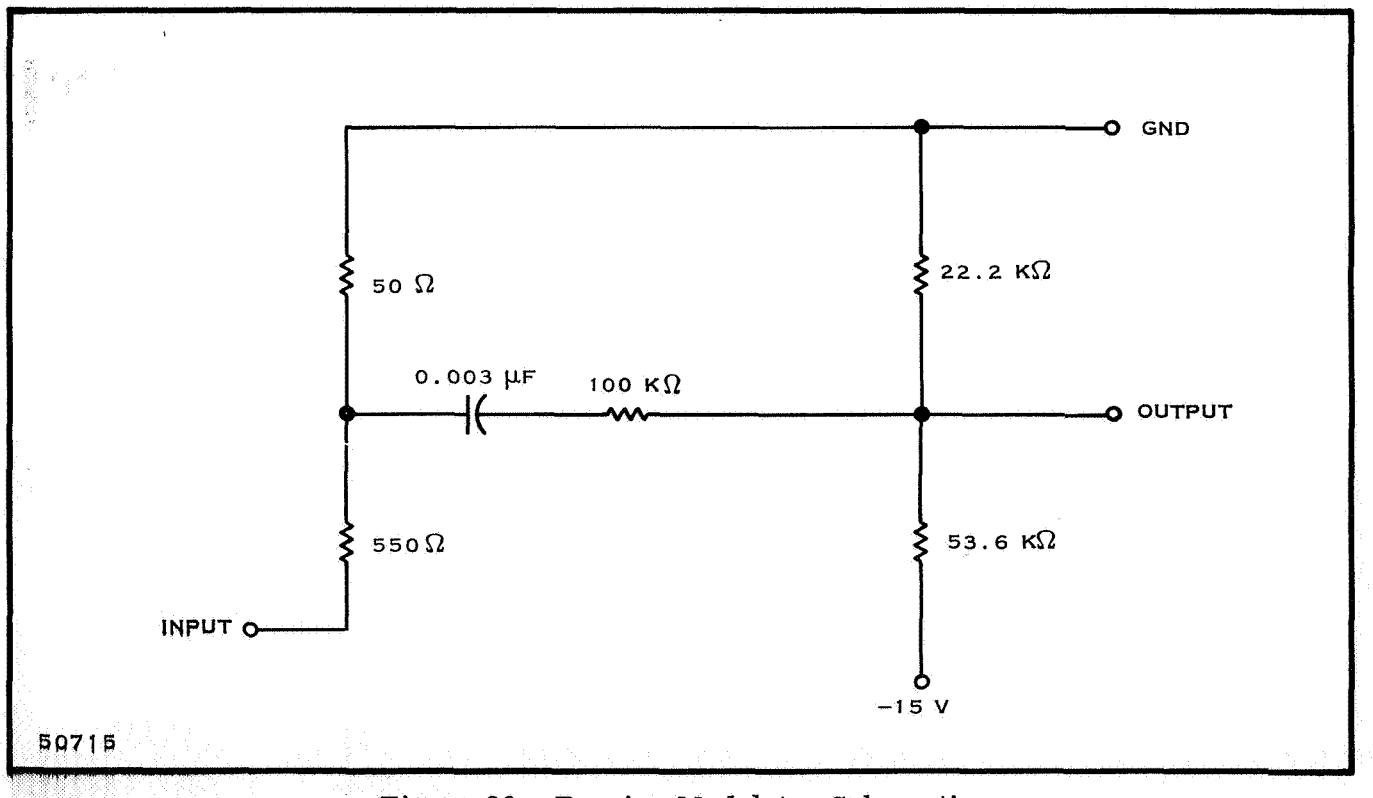


Figure 29. Passive Modulator Schematic

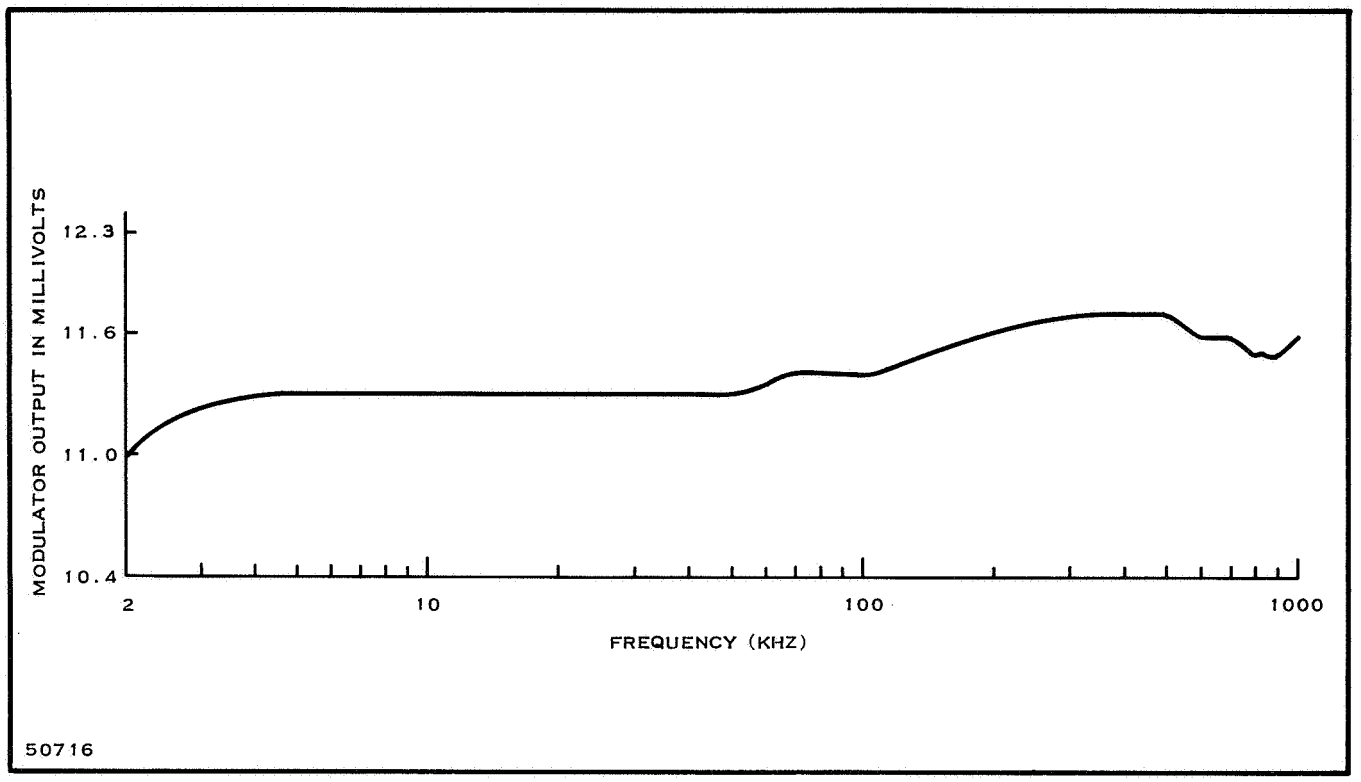


Figure 30. Passive Modulator Output Response

The final modulator circuit contains five elements, four resistors and one capacitor, shown in Figure 31. Its response is shown in Figure 32. For a constant 1VRMS input, the output varied from 15.2 mV to 16.1 mV over the modulation frequency range. The modulator circuitry will be included on the VCO substrate.

The modulator will not be converted to ceramic until the ceramic oscillator has been fabricated and tested. This will allow the complete modulator and VCO to be combined at the same time.

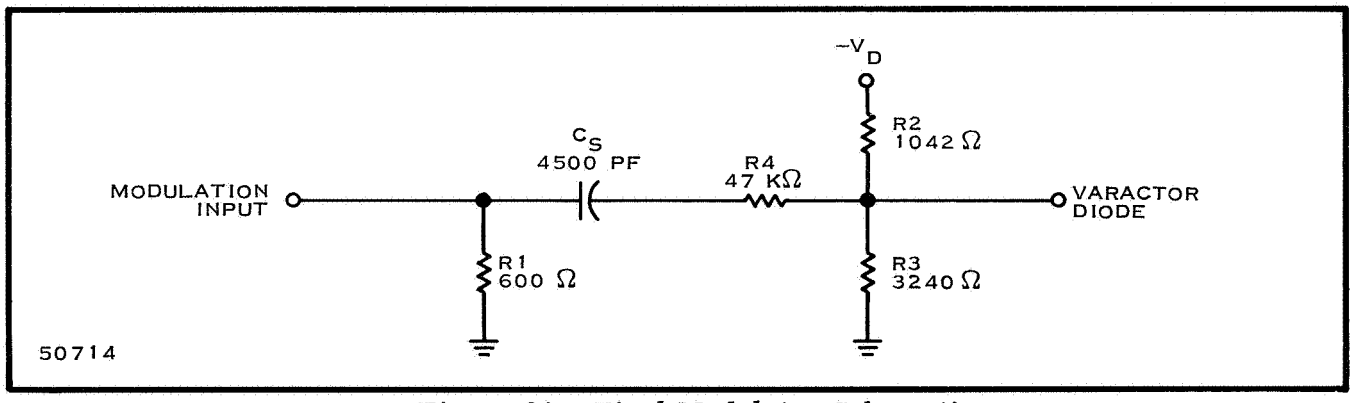


Figure 31. Final Modulator Schematic

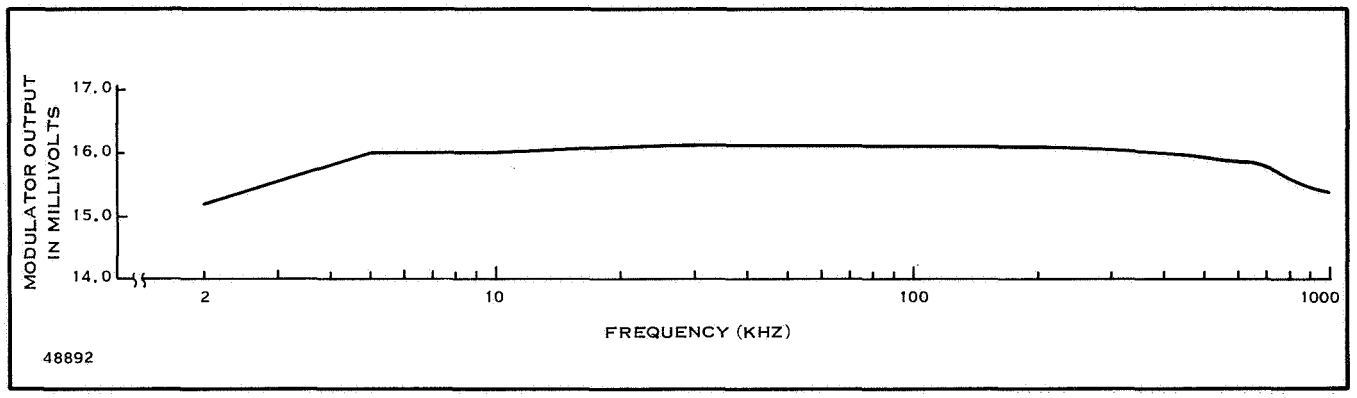


Figure 32. Final Modulator Response

B. POWER AMPLIFIER

1. General

The function of the power amplifier is to increase the level of the 2.25-GHz energy from 30 mW at the output of the VCO to 1 watt minimum at the antenna. The amplifier is broadband to allow use over the 2.2- to 2.3-GHz range without modification.

The design of power amplifiers that yield both efficiency and gain is complicated by nonlinear operation. This precludes the use of general device parameters for the design since the parameters are a function of the device operating point and the output frequency. The design technique has been reduced to the specification of input and output matching networks to match the measured input and output characteristics of the transistor. The device characteristics are measured under the desired conditions of output power, gain and efficiency.

The natural step to integrated microwave transistor amplifiers imposes a minimal size constraint upon the matching network design. Additional constraints such as transistor biasing networks and coupling capacitor dimensions must also be considered.

Since monolithic microwave power amplifiers are not feasible at this stage of technical development, thin-film hybrid fabrication on ceramic substrates will be used. When using these techniques, transmission line matching networks are the most feasible and will be employed. The design of these input and output matching networks has been optimized by the use of an efficient computer program[3]. The matching network problem was reduced to an equivalent nonlinear programming problem by considering the N-filter elements as coordinates in a 2-N dimensional vector space. The optimal solution point in the vector space is found by the use of a "pattern search" routine, which uses randomly chosen orthogonal transformations of the search pattern to minimize an objective function.

For large-signal amplifiers the source and load admittances necessary to match the transistor input and achieve maximum power gain are measured as a func-

tion of frequency at the desired operating levels. The effective transistor input admittance is taken as the complex conjugate of the optimum source admittance. In doing this, it is assumed that the experimental apparatus is lossless.

With the appropriate transistor data, a network configuration is proposed to match the given Y_l to the given Y_s. Proposing a likely network (combination of shorted and open stubs, series line transformation) is a task that becomes easier with practice. The sizes of the lines (Z_o and length) are then adjusted by using the operations research optimization routines to achieve minimum mismatch loss over the frequency range. The routine now in use the "Spider".

To evaluate the merit of one design solution compared with another, a quantity known as "mismatch loss" is evaluated as a function of frequency across the desired band. If a current source I with output admittances Y_s is coupled to a load Y_l, the power delivered to the load is given by

$$P_1 = \left| E_1 \right|^2 R_e(Y_1) \tag{18}$$

$$= \left| \frac{I}{Y_s + Y_1} \right|^2 G_1 \tag{19}$$

Using the maximum power transfer theorem, we know that the maximum power is transferred to the load when

$$Y_1 = Y_s^* = R_e(Y_s) - jI_m(Y_s) \tag{20}$$

and is given by

$$P_{1m} = \left| \frac{I}{Y_s + Y_1} \right|^2 G_1 \tag{21}$$

$$= \left| \frac{I}{Y_s + Y_s^*} \right|^2 G_s \tag{22}$$

$$= \left| \frac{I}{G_s^2} \right|^2 G_s \tag{23}$$

$$= \frac{|I|^2}{4G_s} \tag{24}$$

Then we define the mismatch loss as

$$L = \frac{P_1}{P_{1m}} \tag{25}$$

$$= \frac{4G_s G_1}{|Y_s + Y_1|^2} \tag{26}$$

$$= \frac{4G_s G_1}{(G_1 + G_s)^2 + (B_1 + B_s)^2} \tag{27}$$

The network with the lowest mismatch loss over the desired band of frequencies is the best network.

After choice of configuration, based on the results of the device characterizations, the devices were characterized under the required operating conditions and the required matching networks were optimized, using the computer program described previously. The first breadboard design will be built on 1/16-inch Teflon-filled fiberglass. After the circuit has been optimized on Teflon, it will be scaled to 20-mil ceramic.

2. DEVICE CHARACTERIZATION

a. Dissipation

The transistors selected for use in the power amplifier are from a family of microwave devices recently developed at Texas Instruments. These devices are the L-158A and L-158C (Figures 33 and 34, respectively), selected because they have been used successfully in pulsed applications at 2.25 GHz. However, since all previous data were under pulsed operating conditions, complete device characterization under CW operating conditions was necessary.

Since the characterization of a device is dependent on the output power level, the initial step in characterization was to determine the dissipation limits of the device and its package. In order to determine the dissipation limits, two L-158A devices which would not operate under signal bias were selected for testing. These two devices were subjected to tests, using the test set up shown in Figure 35. The test fixture used to hold the devices, which were mounted in the TI-line package, is shown in Figure 36. Since these devices would not operate under signal bias it was necessary to bias the base-emitter junction in the forward direction by applying a negative voltage to the emitter. The collector voltage was +24 Vdc. The goal of this test was to determine whether the L-158A, mounted in a TI-line package, could dissipate enough heat to allow an RF output power of 1 watt.

The power dissipation tests were not successful. The two devices were destroyed at low power levels while tuning the input and output double-stub tuners; therefore, they were subjected to a failure analysis. Microscopic examination indicated that neither device had been damaged by excessive dissipation but that excessive currents had caused severe burning of the base emitter fingers. It is believed that the excessive currents were caused by low-frequency oscillations induced by the double-stub tuners used for impedance matching.

Since a safe power output limit could not be immediately established, it was decided to limit the output power level to 540 mW and to proceed with the characterization.

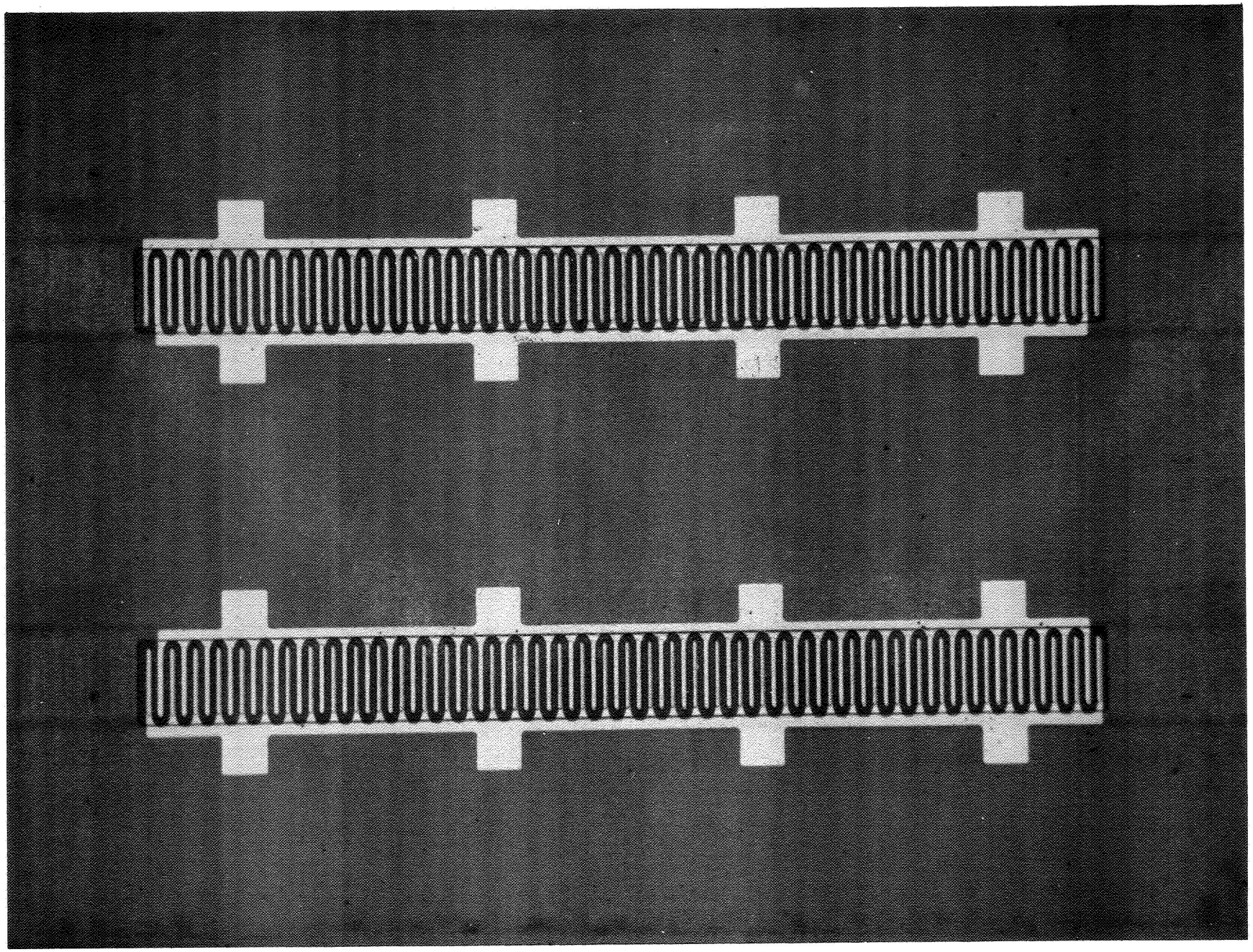


Figure 33. L-158A Geometry

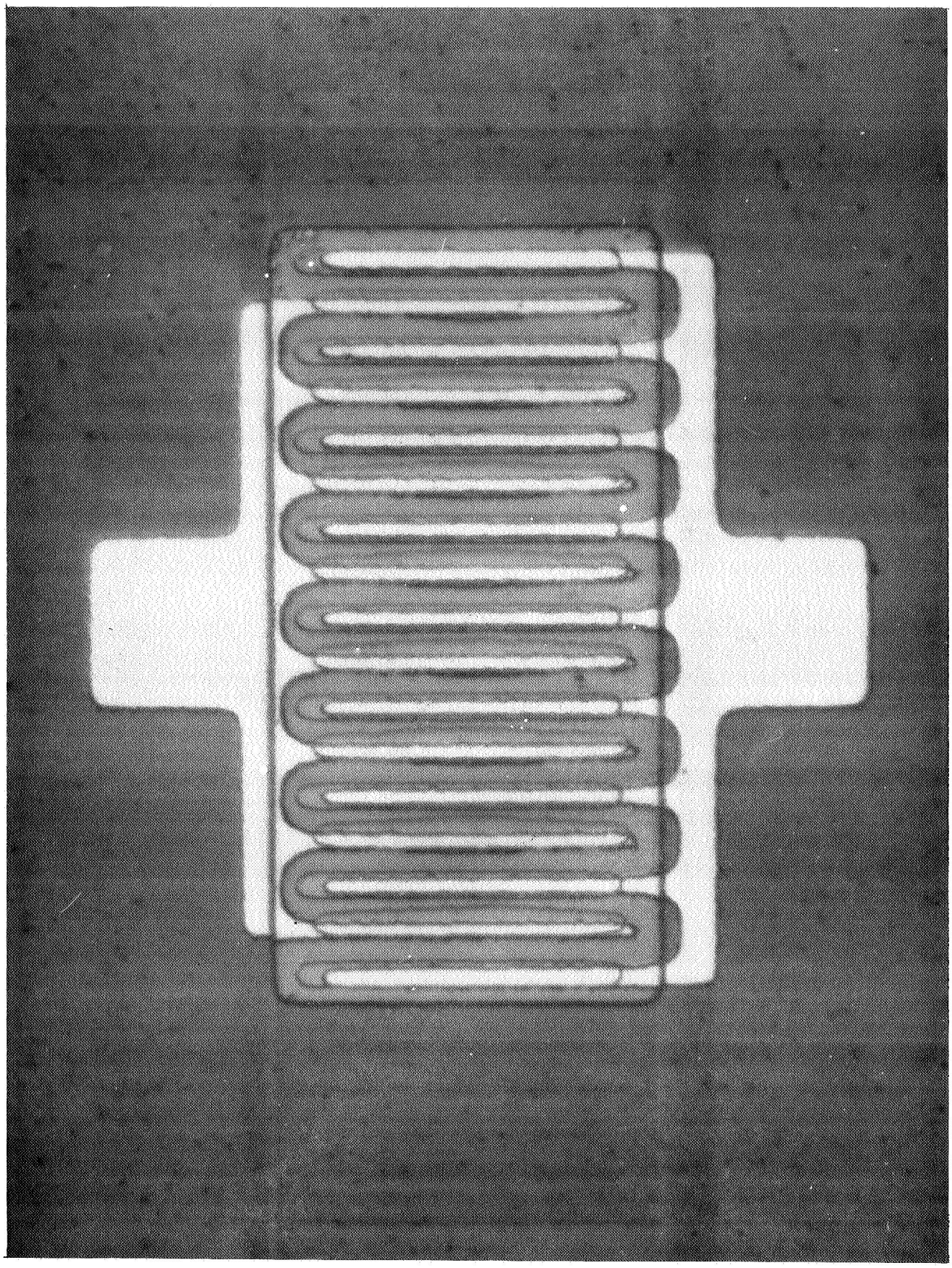


Figure 34. L-158C Geometry

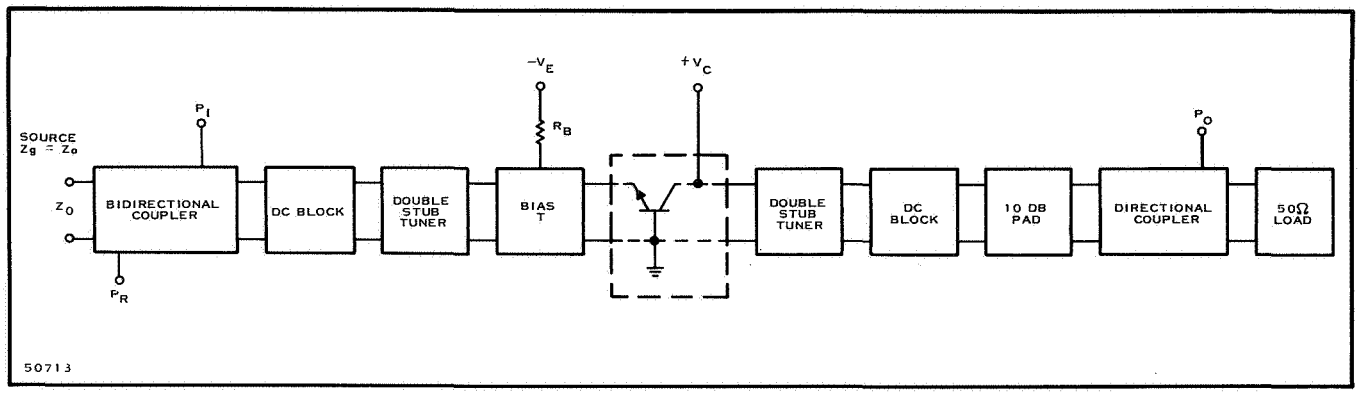


Figure 35. Test Circuit Block Diagram for High Power Dissipation Tests

At a later date another device was subjected to dissipation tests. Since this device would not operate at a collector voltage of +24 Vdc, the voltage was raised to facilitate operation. The test set up is shown in Figure 37. The results of those tests, conducted at 2.25 GHz only, are shown in table VI and are plotted in Figures 38 and 39. The data obtained indicate that the L-158A can deliver a 1-watt RF output. However, since the collector voltage necessary for the 1-watt output is greater than the specification voltage of 24 Vdc, the output power level limit of 540 mW will still be in effect.

Table VI

High Power Dissipation Test

Vc Volts	Pin mW	Pout mW	Ic mA	EFF %	Gain dB
28	410	800	108	26.5	2.90
28	465	900	108	29.8	2.87
28	545	1000	112	31.8	2.64
30	480	1000	112	29.8	3.19
30	555	1100	115	31.9	2.97

b. Configuration

From the results of the dissipation test previously discussed the initial configuration of the power amplifier chain was established as shown in Figure 40. In the parallel configuration each output stage will be required to deliver 540 mW. This allows 80 mW to be used for losses in the power-combining network and another portion of the output to be sampled for AFC purposes. The final stage L-158A devices and the driver stage L-158C devices will be operated class C. A buffer amplifier L-158C device will be used between the VCO output and the driver stages, operating class A to assure a reasonably constant load to the VCO.

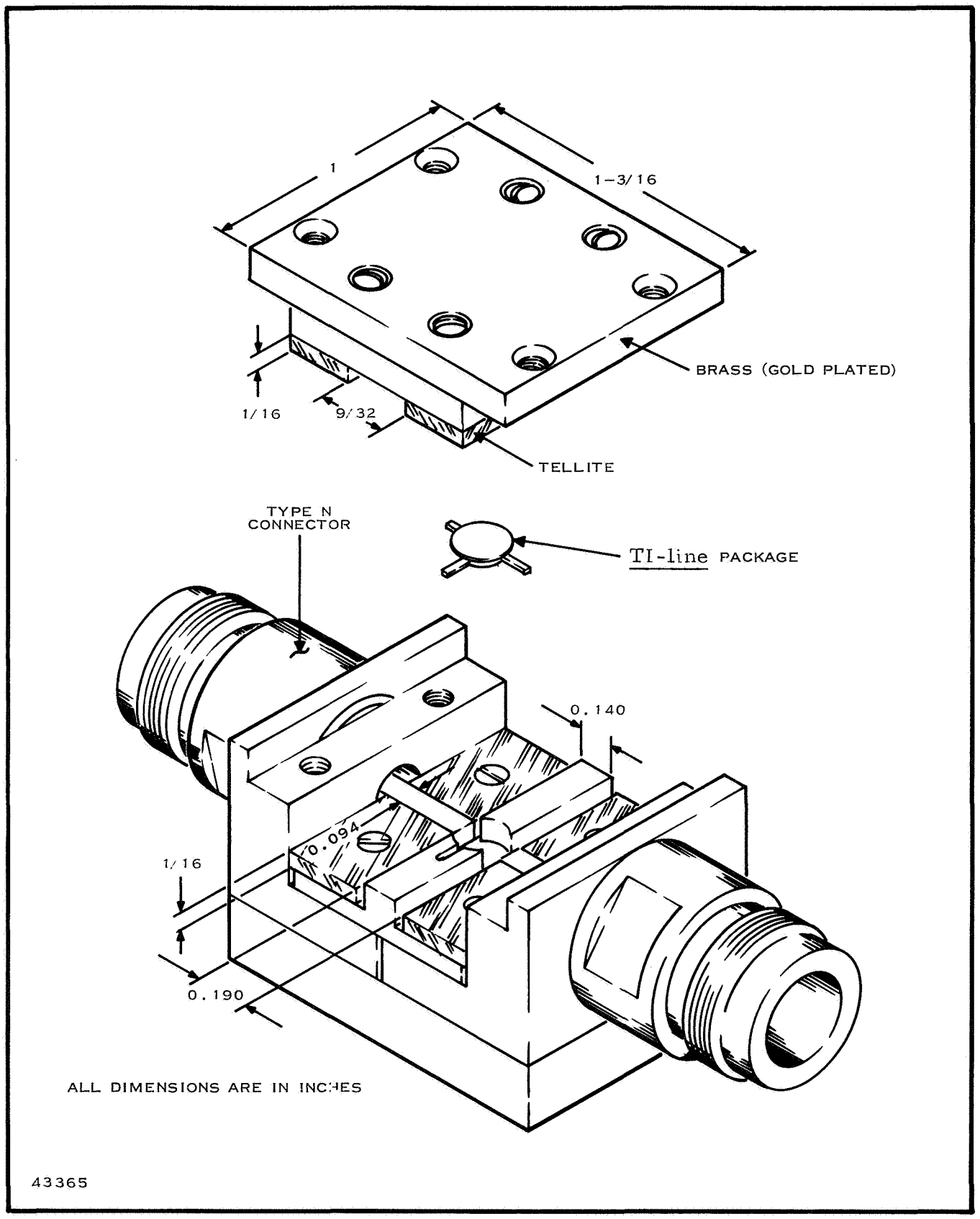


Figure 36. Improved TI-line Mount

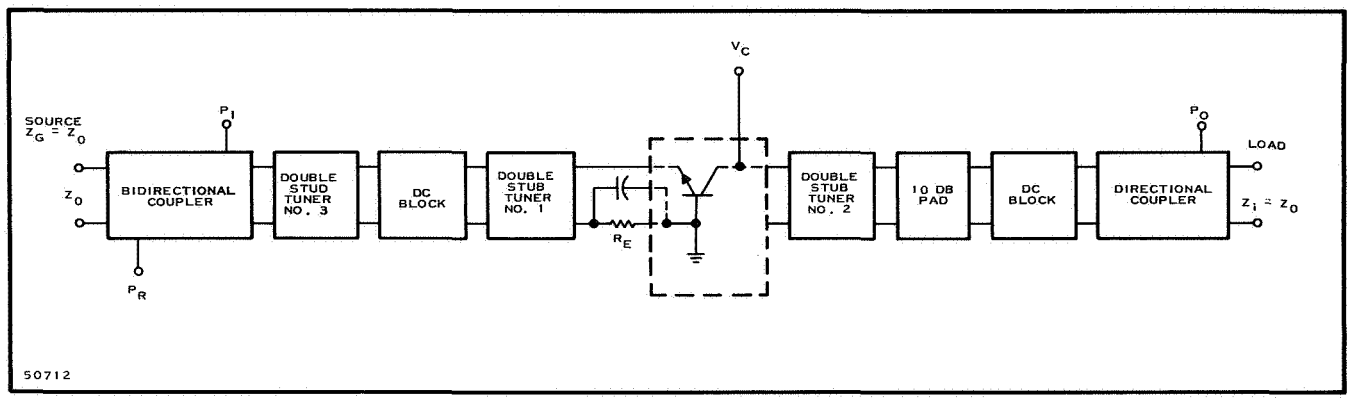


Figure 37. Class C Characterization Test Circuit Block Diagram

High-power investigations will be continued and, should the results prove favorable, a single amplifier chain design will be used. One possible configuration is shown in Figure 41.

c. Admittance Parameters

Once the output operating level of a device has been established, characterization can be accomplished. For small-signal operation, it is possible to characterize a transistor by a set of admittance or impedance parameters or by a sufficiently complete equivalent circuit. From this information the designer can derive the appropriate input, output and interstage coupling networks to give the desired performance. The problem is complicated considerably with large-signal operation, as the parameters of the transistor vary with signal level. Large-signal analysis of transistors has, unfortunately, been developed only for the low-frequency case where parasitics are not considered and the frequency of operation is several orders of magnitude below the maximum capabilities of the device. At any given power lever, however, it is possible to determine the optimum source and load admittances by direct performance measurements in a flexible test amplifier arrangement.

Figures 37 and 16 are block diagrams of the test arrangements used in characterization, which is accomplished by selecting the desired dc operating bias conditions and frequency, and then adjusting the variable tuning networks - double stub tuners - to obtain maximum gain while maintaining a minimum of reflected power at the input (less than 10 percent, in order to be considered a valid measurement). After this optimum adjustment is made, the source and load admittances are measured, using the slotted line technique. Since the electrical lengths of the fixture are known quite accurately, the source and load admittances can be transformed to the transistor package. If the admittances are to be measured at the transistor chip itself, the value measured at the terminals of the package may be transformed by using the equivalent circuit of the package. Figure 42 shows the approximate electrical equivalent circuit of the TI-line microwave package.

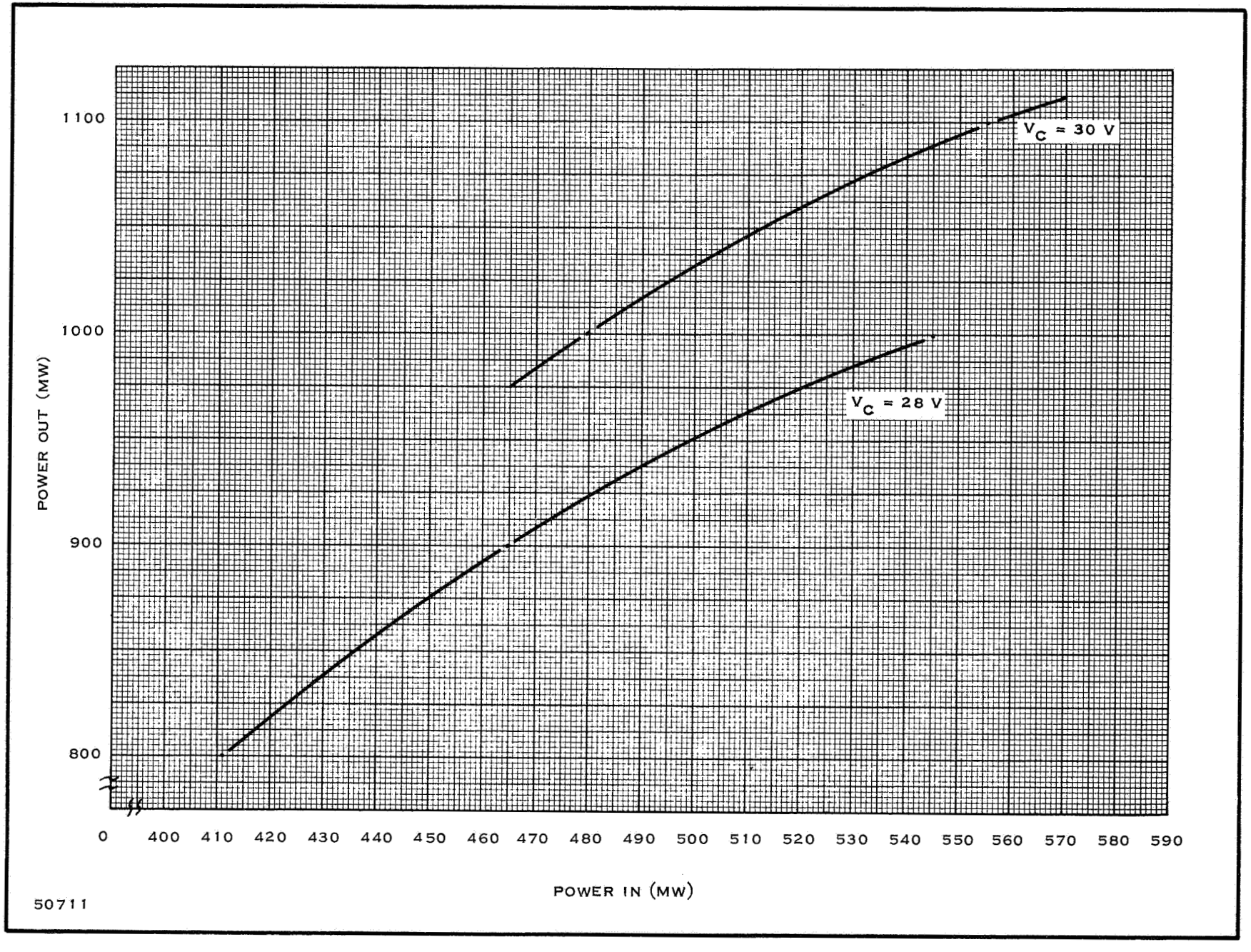


Figure 38. Power Out Versus Power In

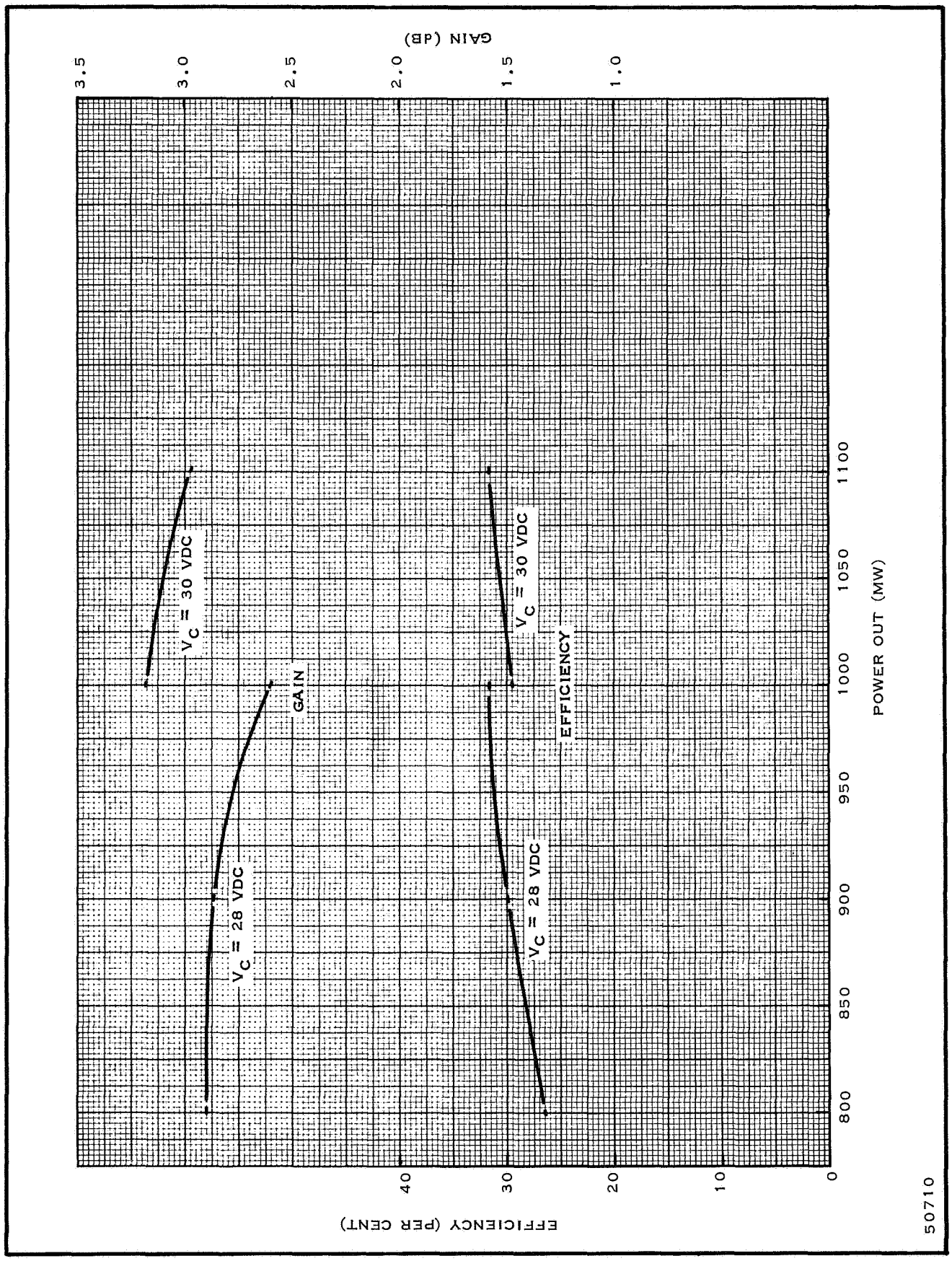


Figure 39. Gain and Efficiency Versus Power Output

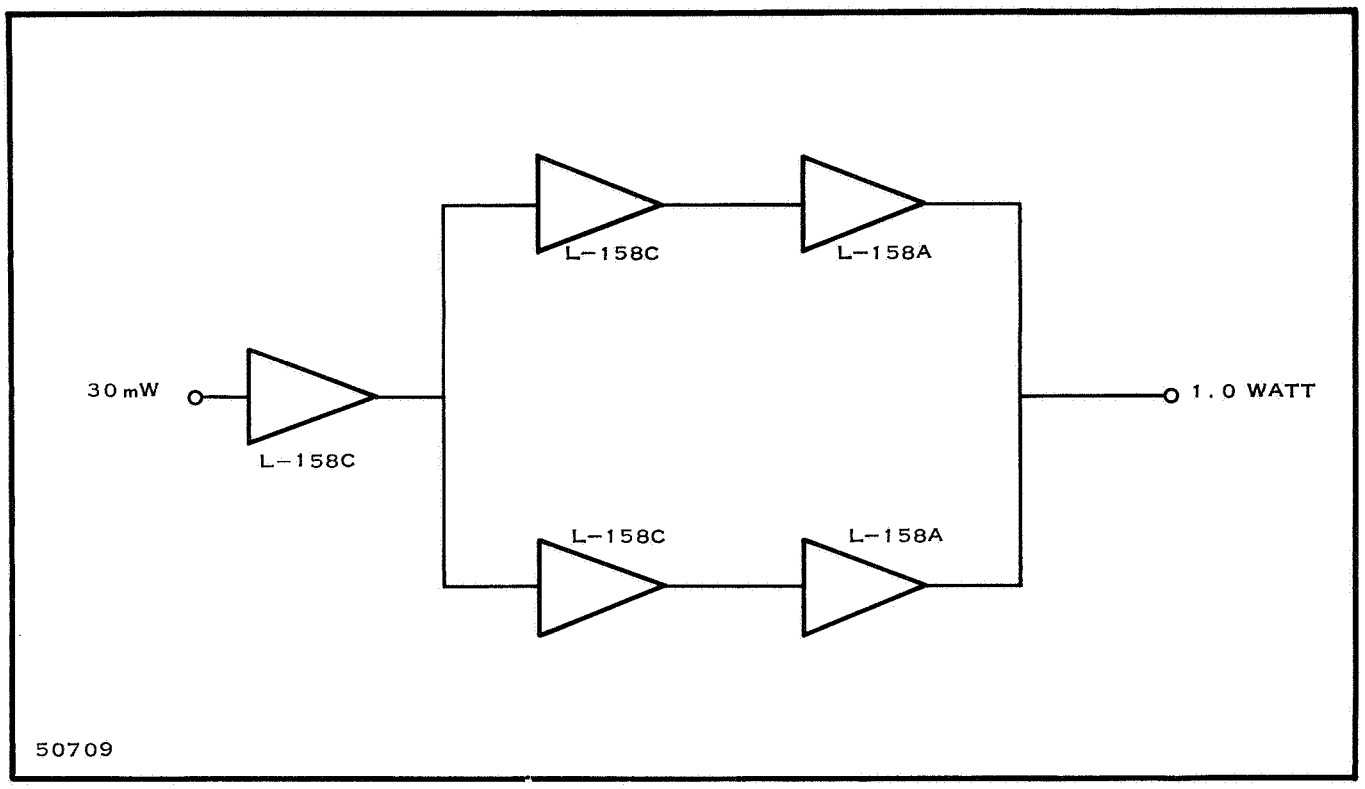


Figure 40. Parallel Path Amplifier Configuration

The first device to be characterized was an L-158A, No. A-3. The test arrangement used is shown in Figure 37, with the exception that the emitter resistor R_E was not in the circuit. The device was characterized under two different operating conditions: first, with the device tuned for maximum gain, and second, with the amplifier tuned for minimum reflected power at the input and the double-stub tuner No. 2 (DST No. 2) adjusted to give the required 540-mW output power. At maximum gain the device was very regenerative, but under minimum reflected power conditions the regeneration was reduced to a minimum. Due to the common-base mounting configuration, regeneration will always be present. The data obtained from device No. A-3 under the foregoing conditions are shown in Table VII.

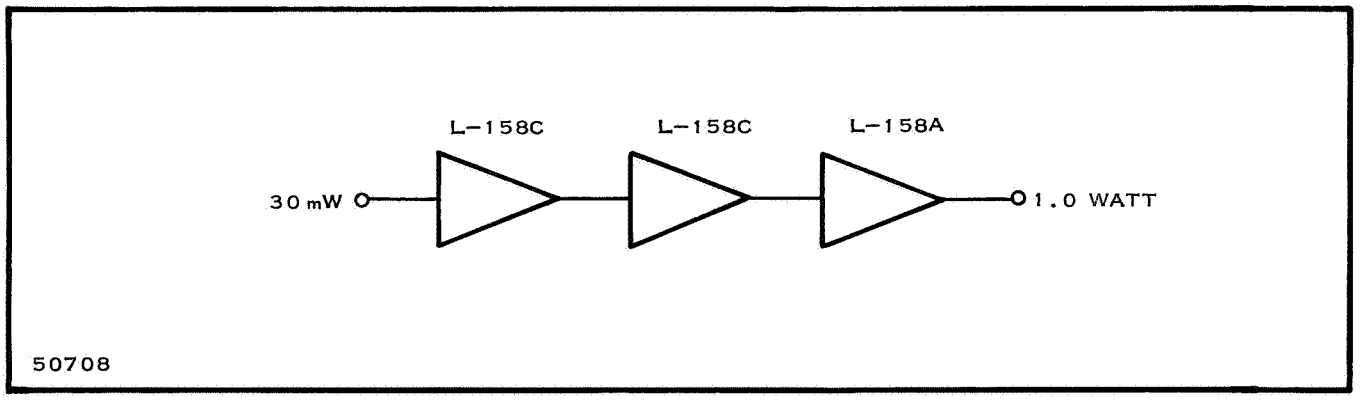


Figure 41. Single Path Amplifier Configuration

Table VII

L-158A Device No. A3 Initial Characterization Data, Class C

Condition	Freq. GHz	Power In(mW)	Power Out(mW)	Reflected Power (mW)	Collector Current (mA)	Gain dB	Efficiency dc to RF %	Y_{in} millimhos	Y_{out} millimhos
Max Gain	2.2	140	540	2.8	105	5.76	21.4	34.0-j94.0	6.0 +j34.0
	2.25	165	540	5.8	103	5.15	21.9	58.0-j78.0	13.0+j33.0
	2.3	248	540	2.4	102	3.37	22.1		
Min Ref. Pwr.	2.2	160	540	2.2	94	5.28	24.0	44.0-j110.0	9.6+j35.6
	2.25	210	540	1.6	80	4.1	28.1	70.0-j62.0	15.0+j29.0
	2.3	265	540	2.1	94	3.1	24.0	42.0-j112.0	12.0+j37.0

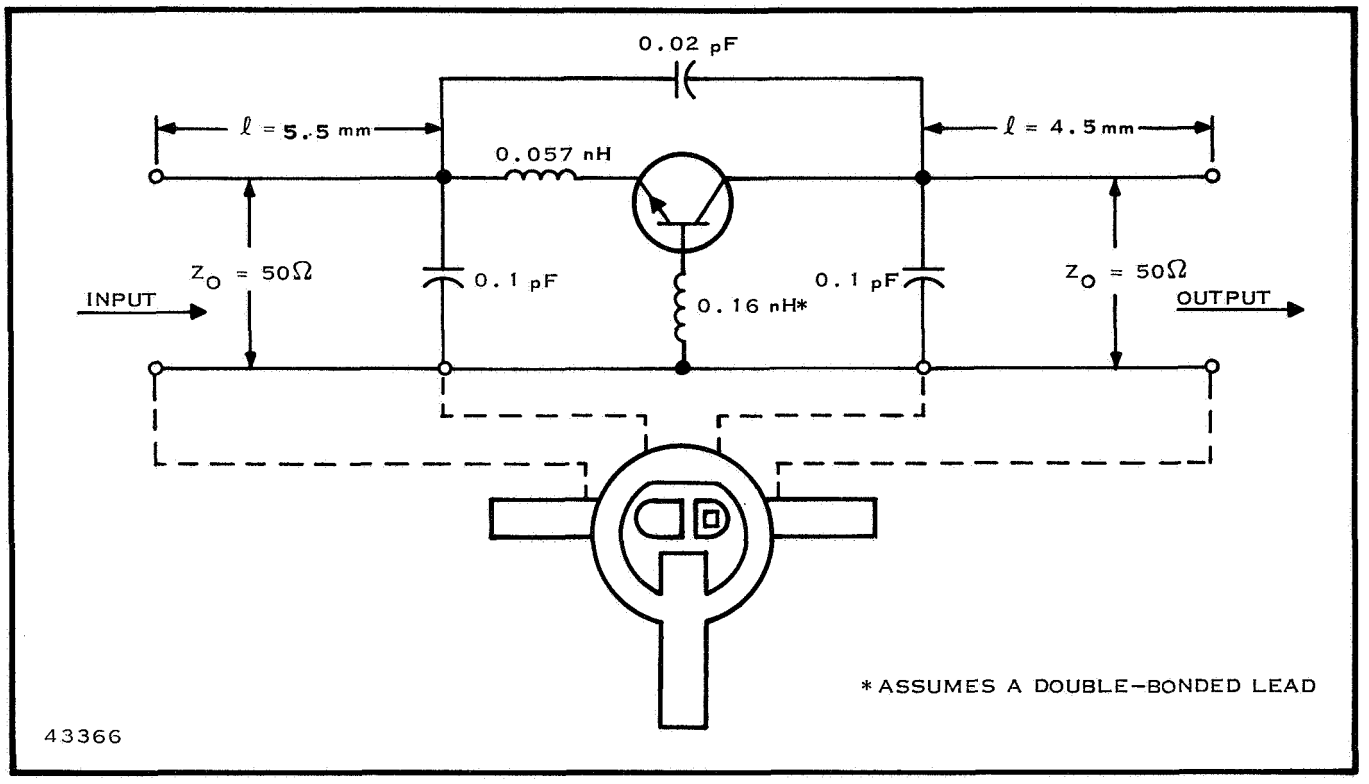


Figure 42. TI-line Package and Approximate Equivalent Circuit

In attempting to characterize more L-158A devices, two were destroyed before any useful data were obtained. In order to provide additional protection for any future devices, a resistor was placed in the emitter leg of the amplifier. Bypassing of this resistor is accomplished through the physical construction of the mount. As can be seen from table VIII, a comparixon of the gain and efficiency of device No. A3 with and without R_E, the addition of R_E reduced the gain roughly 1 dB. However, with the addition of R_E the amplifier could be tuned for maximum gain and minimum reflected power at the same time.

Table VIII

Effect of Emitter Resistor R_E

Frequency GHz	With R_E		Without R_E	
	Gain dB	EFF %	Gain dB	EFF %
2.2	3.77	22.5	5.28	24
2.25	3.22	23.4	4.1	28.1
2.3	2.45	24.1	3.1	24.0

Three more L-158A devices were characterized and the resulting data are shown in table IX (device No. A3 data are also included in this table).

With the input drive to the L-158A devices determined, the output power of the driver amplifier was established. The device selected for the driver is the L-158C, and it will be operated class C. The characterization data for class C operation are shown in Table X.

It is of interest to note that the L-158C device, No. 7, was capable of producing the required 540 mW output with good gain (3.7 dB) and adequate efficiency (38 percent). Assuming that the heat dissipation of the ceramic hybrid circuit is adequate, the L-158C could be used in the final output stages or to drive the L-158A to a 1-watt output, if this becomes feasible. Further device characterization of the L-158C at high-output power levels will be conducted.

Since the load presented to the output of the VCO needs to be relatively constant, an L-158C device, operating class A, will be used as a buffer amplifier. The characterization results are shown in Table XI.

At this point a sample calculation will be performed to determine the admittance parameters of a device. The calculation will be performed at 2.25 GHz only, for an L-158C device (No. 7), operating class C.

To determine Y_{in} and Y_{out} the amplifier must first be tuned for the desired operation. Once tuning is accomplished, the TI-line mount (Figure 36) with the device is removed from the test circuit (Figure 37). Using a slotted line, the VSWR and its associated voltage minimum looking into DST No. 1 and DST No. 2 measured:

(DST No. 2) $\rho_{out} = 7.1$ $E_{min} = 239.1$

(DST No. 1) $\rho_{in} = 12.2$ $E_{min} = 212.0$

A short is then placed on the slotted line and the voltage minimum points on both sides of the previously measured minimums are recorded:

$$E_{min_1} = 194.6$$

$$E_{min_2} = 261.2$$

The frequency wavelength is determined by

$$\lambda = 2(E_{min_2} - E_{min_1})$$

$$= 2(261.2 - 194.6)$$

$$= 133.2\text{mm}$$

Table IX

L158A Characterization Data, Class C

Device No.	Frequency (GHz)	Power In (mW)	Power Out (mW)	Power Reflected (mW)	V_c volts	Ic (mA)	Gain dB	EFF %	Y_{in} millimhos	Y_{out} millimhos
A3	2.20	227	540	0.5	24	100	3.77	22.5	40.0-j95.0	6.4+j34.4
	2.25	257	540	0.25	24	96	3.22	23.4	57.6-j78.0	11.6+j32.2
	2.3	330	580	2.8	24	100	2.45	24.1	55.0-j81.0	11.2+j35.0
A22	2.2	235	540	0.005	24	94	3.62	23.9	45.0-j102	9.4+j34.0
	2.25	282	540	0.34	24	90	2.82	25.0	62.0-j91	8.6+j34.0
	2.30	331	550	1.0	24	93	2.12	24.6	60.0-j90	10.6+j35.0
2	2.20	254	540	0.35	24	68	3.28	33.7	16.4-j74.0	9.0+j35.0
	2.25	212	540	0.05	24	93	4.06	24.6	19.0-j78.0	8.6+j36.4
	2.30	288	540	0.04	24	96	2.73	23.4	20.0-j70.0	9.0+j39.0
1	2.2	250	620	0.14	24	89	3.94	25.3	19.0-j76.0	9.0+j36.6
	2.25	250	540	0.05	24	82	3.35	27.4	22.0-j78.0	9.0+j35.0
	2.30	340	540	0.05	24	91	2.01	24.8	19.0-j72.0	9.6+j38.8

Table X

L-158C Characterization Data, Class C

Device No.	Frequency (GHz)	Power In (mW)	Power Out (mW)	Power Reflected (mW)	V_c volts	Ic (mA)	Gain dB	EFF %	Y_{in} millimhos	Y_{out} millimhos
21	2.20	60	270	0.9	24	32	6.5	35.2	30.0-j64.0	3.2+j8.2
	2.25	59	270	0.74	24	30	6.6	37.5	40.0-j60.0	3.8+j9.8
	2.30	66	270	1.6	24	34	6.1	33.1	32.0-j62.0	4.6+j9.6
5	2.20	107	380	0.22	24	48	5.5	33.0	28.0-j52.0	3.2+j10.2
	2.25	107	360	0.36	24	43	5.3	34.9	38.0-j46.0	4.2+j10.0
	2.30	107	340	0.32	24	38	5.0	37.2	26.0-j58.0	3.8+j10.8
7	2.20	110	340	2.5	24	37	4.9	38.3	38.0-j78.0	3.6+j10.6
	2.25	115	340	0.24	24	36.5	4.7	38.6	34.0-j78.0	3.6+j10.8
	2.30	140	340	1.3	24	35	3.8	40.5	42.0-j74.0	4.2+j10.8
	2.20	175	540	2.9	24	51	4.9	44.2	38.0-j78.0	3.6+j10.6
	2.25	186	540	2.4	24	47	4.6	47.9	34.0-j78.0	3.6+j10.8
	2.30	227	540	2.8	24	49	3.7	45.9	42.0-j74.0	4.2+j10.8

Table XI

L158C Class A Characterization Data

Device No.	Frequency (HGz)	Power In (mW)	Power Out (mW)	Power Reflected (mW)	V_c volts	Ic (mA)	Ve volts	Ie (mA)	Gain dB	EFF %	Y_{in} millimhos	Y_{out} millimhos
21	2.20	30	242	0.05	24	23	-5.4	25	9.1	38.8	24.0-j42.0	4.0+j7.4
	2.25	30	255	0.03	24	23	-5.4	25	9.3	40.9	20.0-j42.0	3.8+j7.8
	2.30	30	234	0.1	24	23	-5.4	25	8.9	37.6	21.0-j37.0	4.2+j8.0
5	2.2	NO DATA-UNIT DESTROYED WHILE TUNING AT 2.2GHz										
	2.25	30	251	0.08	24	25	-6.4	28	9.2	35.4	17.0-j39.0	1.8+j8.8
	2.30	30	289	0.09	24	26	-6.4	28	9.0	33.8	14.0-j36.4	1.9+j9.2
7	2.2	30	260	0.06	24	30	-7.4	32	9.4	31.7	14.4-j41.6	2.0+j10.5
	2.25	30	273	0.1	24	30	-7.4	32	9.5	33.3	16.0-j42.0	1.8+j8.6
	2.30	30	259	0.09	24	30	-7.4	32	9.3	31.6	12.0-j43.0	1.9+j9.8

To determine the shift of the minimum in wavelengths

$$\text{Input: } \Delta\lambda = (212.0-194.6)/133.2 = 0.1306\lambda$$

In the test setup, the slotted line reference of 0.0 mm is located at the generator end and the 450-mm reference is located at the load end. Therefore, the direction of the minimum shift of the input is toward the generator when the short is placed on the slotted line.

Similarly,

$$\text{Output: } \Delta\lambda = (261.2 - 239.1)/133.2 = 0.1659 \text{ toward the load}$$

At this point the impedance looking into the stubs can be determined. On the Smith Chart of figure 43 a circle is constructed which corresponds to a VSWR of 12.2. Starting at the short on the Smith Chart and rotating 0.1306 wavelengths toward the generator, point 1 on the Smith Chart is located.

Since the impedance (or admittance) of the device must be measured, the impedance measured at the stubs must be transformed to the input of the TI-Line package (shown by the outer pair of dashed lines in Figure 42). This length, the distance between the measurement reference plane of the double-stub tuners and the edge of the TI-line package located in the mount, is measured and found to be 0.335 λ at 2.25 GHz.

Rotating 0.335 λ from point 1 toward the generator determines point 2, which is the load impedance at the input of the TI-line package. The corresponding admittance can be determined by proceeding to point 3, which is diametrically opposite point 2. Since the device was characterized under maximum power transfer, the device admittance is equal merely to the conjugate of the load admittance. In order to find the absolute admittance it is necessary to multiply the Smith Chart readings by 20 X 10^{-3} mhos (50 ohms), since it is to this that the measuring system is referenced. A similar procedure is used to determine the output admittance. The Smith Chart used for the output admittance is shown in Figure 44.

$$Y_{out} = (0.18 + j.54)\ 20 \times 10^{-3}$$

$$= 3.6 + j10.8 \text{ millimhos}$$

$$Y_{in} = (1.7 - j3.9)\ 20 \times 10\text{-}3$$

$$= 34 - j78 \text{ millimhos.}$$

3. Power Dividing and Combining Networks

Because of the parallel amplifier configuration it is necessary to use a power divider network at the output of the buffer amplifier and a power combining network at the outputs of the final amplifiers. For simplicity, both of these networks will be designated as power dividers.

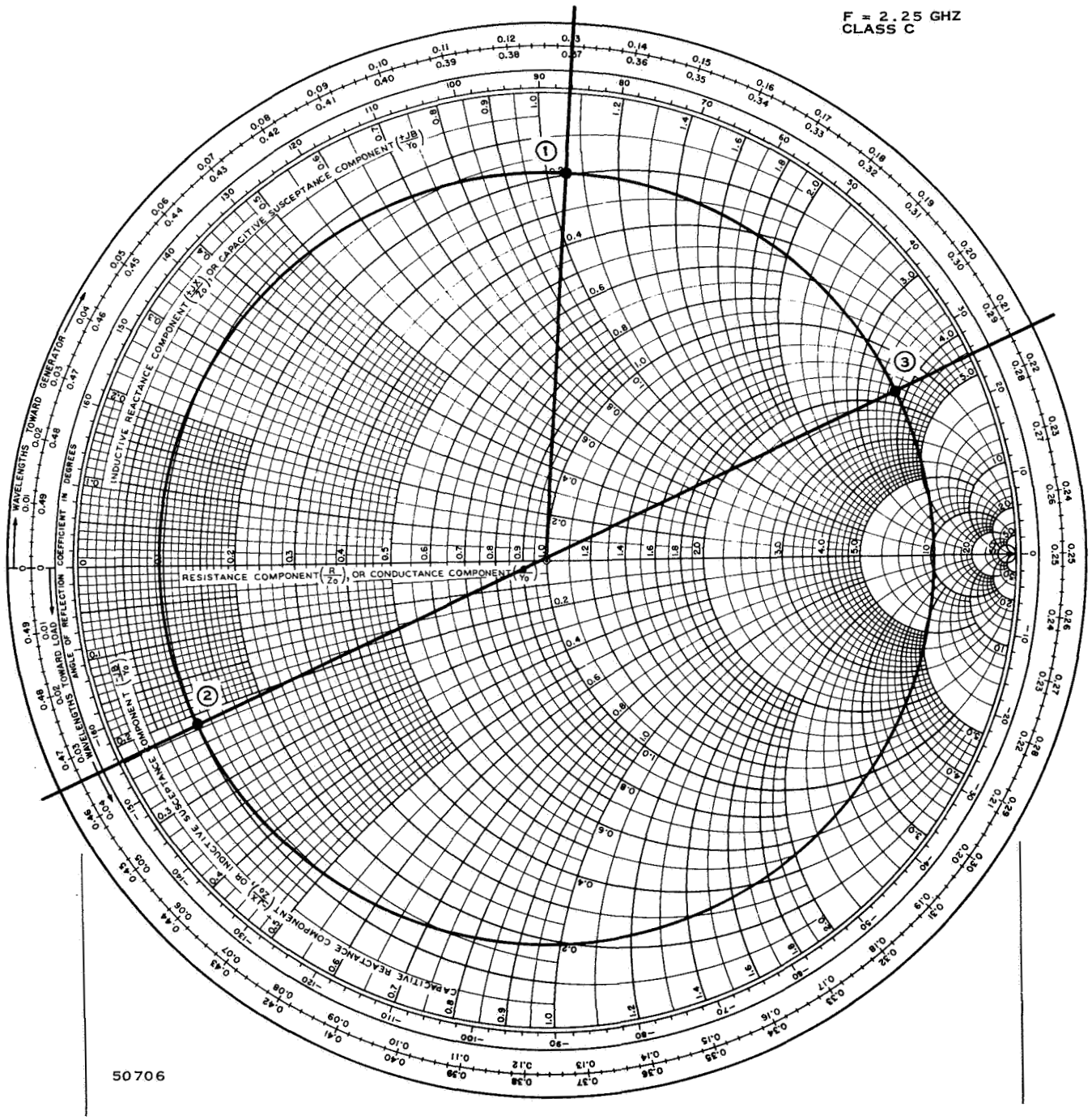


Figure 43. Y_{in} L-158C Device No. 7

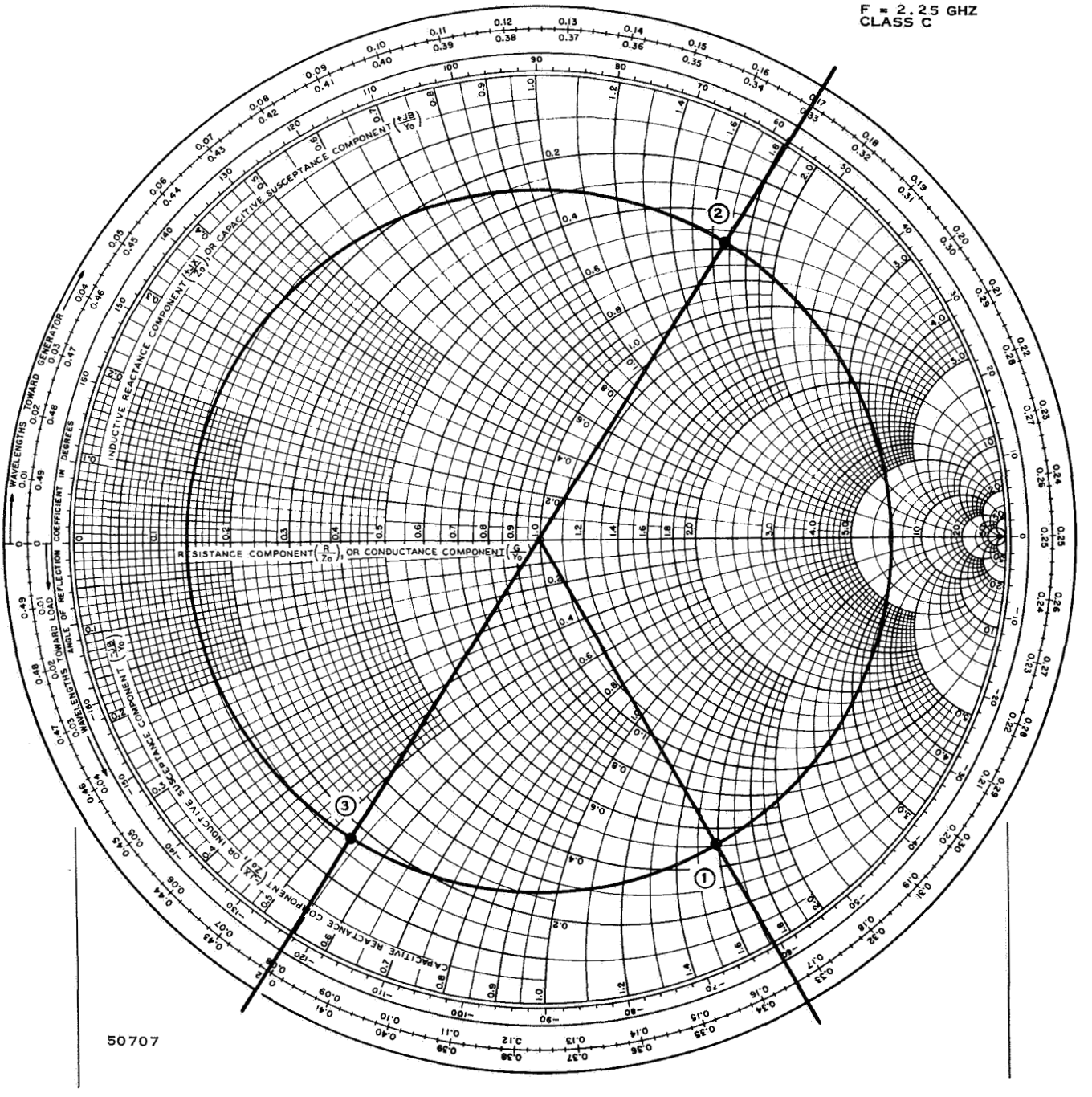


Figure 44. Y_{out} L-158C Device No. 7

The power divider network to be used at the outputs of the buffer and final power amplifiers is a combination N-way and reactive power divider. The rigorous mathematical derivation of the design is the same as the split-tee power divider described by Parad and Moynihan.[8] An investigation of this divider has been made at Texas Instruments. Only the basic outline of the derivation and the results will be given here for equal power division for a two-port output.[1,2]

The power divider is constructed using N 1/4-wavelength sections of line, with each section having a characteristic impedance equal to the geometric mean of the two impedances to be matched. N resistors are connected from a common tie point "P" to the line sections 1/4-wavelength from the input junction, to achieve the isolation properties (the only function of the resistors).

The specifications for the general power divider (Figure 45) are:

1) N outputs with a specified power division
2) All ports matched
3) Isolation between outputs
4) Input port isolated from the resistors (the resistors dissipate no input signal power).
5) Equal phase outputs

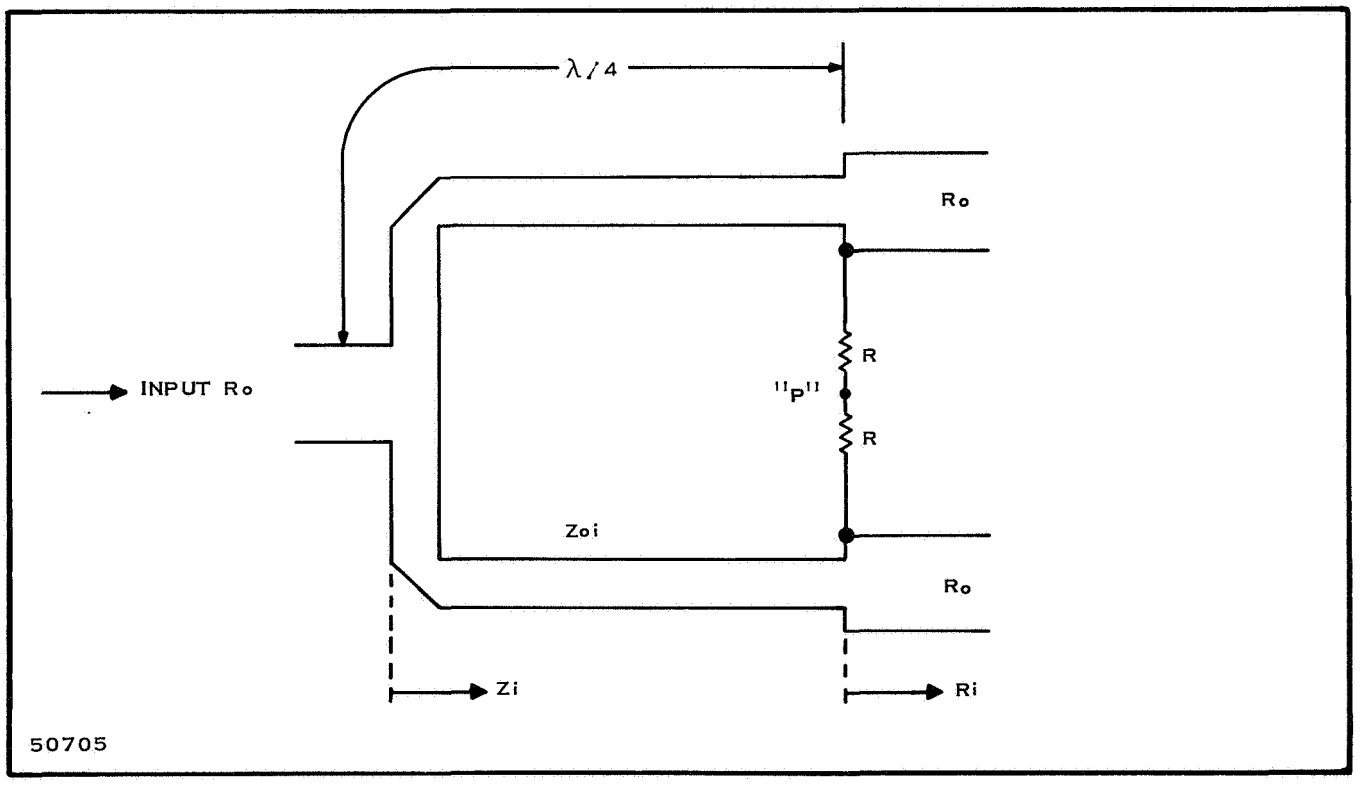


Figure 45. Power Divider

From specification (4), the voltage at all the points of R_i must be equal when power is fed to the input port. (R_i is the output resistance, as seen from these junctions.)

If the power division required by specification (1) are expressed by the output powers P_1, P_2 ---P_n and the output resistances at the middle junction are R_i, then the voltage at the points of R_i can be expressed by

$$V_i = \sqrt{P_i R_i}$$

and is constant for all i's. Therefore

$$R_1 = \frac{V_i^2}{P_i} \quad , R_2 = \frac{V_i^2}{P_2} , \bullet \bullet \bullet R_i = \frac{V_i^2}{P_i} \tag{28}$$

From this it can be seen that the value of R_i must be adjusted to be inversely proportional to the power emerging from the port.

For the particular case in which we are interested

$$N = 2$$

$$P_i = \frac{P_s}{2}$$

where P_s is the power fed to the input port

$$R_i = R_0$$

and some simplifications can be made.

After knowing the resistances R_i, the characteristic impedance of the 1/4-wave transformers at the input can be determined by imposing the input match specification (2) and the power division specification (1). At each input junction the voltage is defined as V. The input impedance of each section is:

$$Z_i = \frac{Z_{01}^2}{R_i} \tag{29}$$

and is purely resistive. If the power P_i is to travel to the i^{th} port, then from

$$P_i = \frac{V^2}{Z_i}$$ we obtain

$$Z_1 = \frac{V^2}{P_i}$$

$$Z_2 = \frac{V^2}{P_2} \bullet \bullet \bullet$$

$$Z_i = \frac{V^2}{P_i} \tag{30}$$

The input match condition can be expressed as

$$Y_{in} = \frac{1}{R_0} = \frac{1}{Z_1} + \frac{1}{Z_2} + \bullet \bullet \bullet \frac{1}{Z_i} \tag{31}$$

Substituting equation (30) into equation (31) we get

$$\frac{1}{R_0} = \frac{P_1 + P_2 + \bullet \bullet \bullet P_n}{V^2} \tag{32}$$

Solving for V^2

$$V^2 = R_0 \sum_{i=1}^{i=n} P_i = R_0 P_s \tag{33}$$

Substituting equation (33) into equation (30) yields

$$Z_i = R_0 \frac{P_s}{P_i} \tag{34}$$

Rearranging equation (29) and substituting equation (34) into (29) we get:

$$Z_{0i} = \sqrt{Z_i R_i}$$

$$Z_{0i} = \sqrt{R_0 R_i \frac{P_s}{P_i}}$$

Since $R_i = R_0$

$$Z_{0i} = R_0 \sqrt{\frac{P_s}{P_i}} \tag{35}$$

Therefore, for $\frac{P_s}{P_i} = 2$ for a two-port output we get

$$Z_{0i} = R_0 \sqrt{2} \tag{36}$$

The design of the power divider is now complete except for the value of the isolation resistors. When one of the output ports is energized, the voltage fed through the resistances must be equal in amplitude and 180 degrees out of phase with that fed through the transformers and input junction to each individual output port. The calculation of the values of the isolating resistors is complex but it can be shown that the values of the resistances are equal to R_1, the output resistance at the junction where the resistor is connected.[2]

Since $R_i = R_0$

$$R_{(\text{isolations})} = R_0$$

The design of the power divider is now complete and is shown in Figure 46.

The values of R_0 to be used in the output power divider need to be determined. The overall power divider configuration (the divider itself and matching networks to the input and output impedances) can take on two different forms, as shown in Figure 47.

In Figure 47A the output impedance of the transistor chip is rotated through some length of transmission lines until it is purely resistive and is R_0. At this point the power divider is entered, with its characteristic impedance set by the magnitude of R_0. A matching section is used at the output to transform R_0 to the required 73-ohm output.

In Figure 47B the power divider R_0 is set to 73 ohms and two matching sections are used to match the two chip devices to the input of the divider.

The configuration in Figure 47A appears to be the simpler of the two; because it uses only one matching section, it is investigated first. All calculations are performed at a frequency of 2.25 GHz.

The average dynamic output admittance Y_{out} of the final power amplifiers is $0.50 + j\,1.66$, normalized to 20×10^{-3} mhos. This admittance, located on the

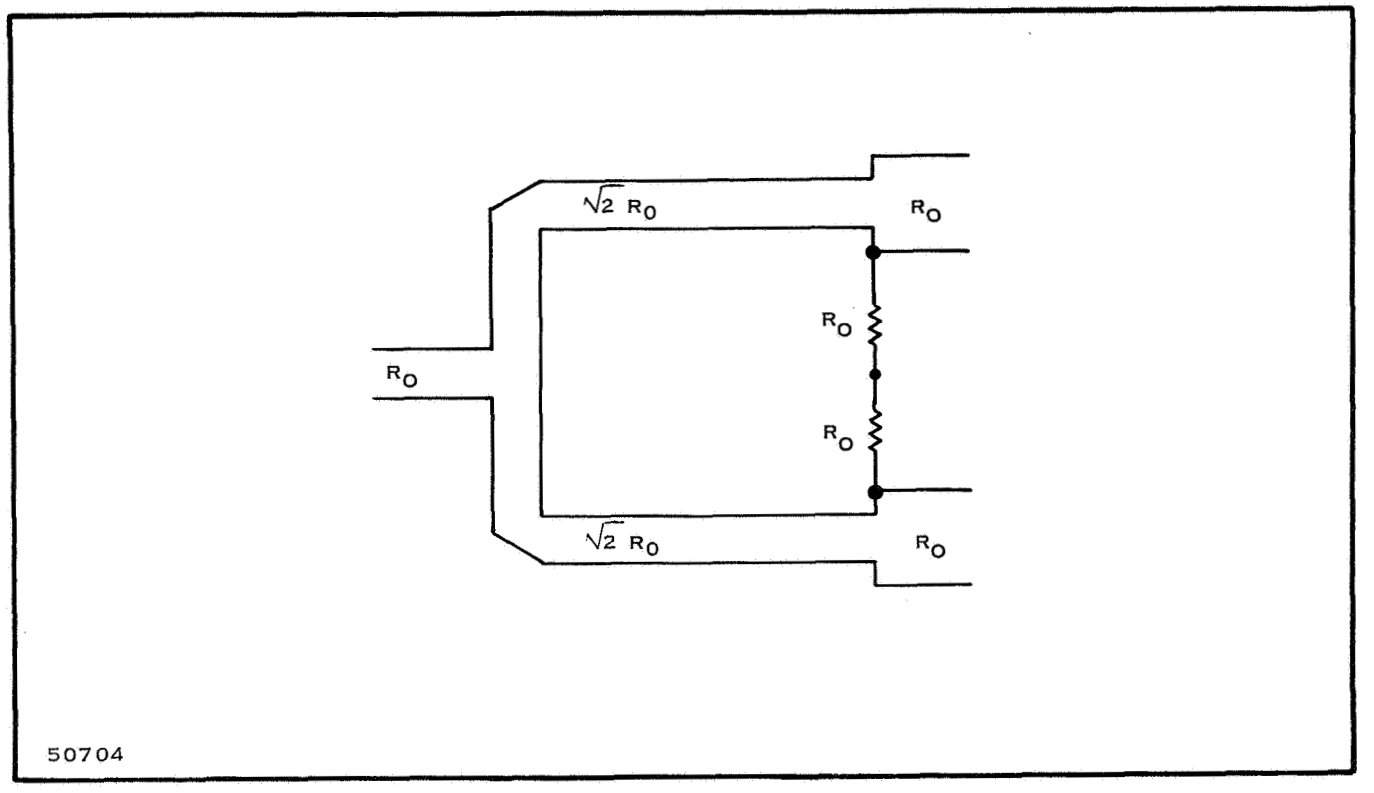


Figure 46. Power Divider Impedances for Two-Output Parts

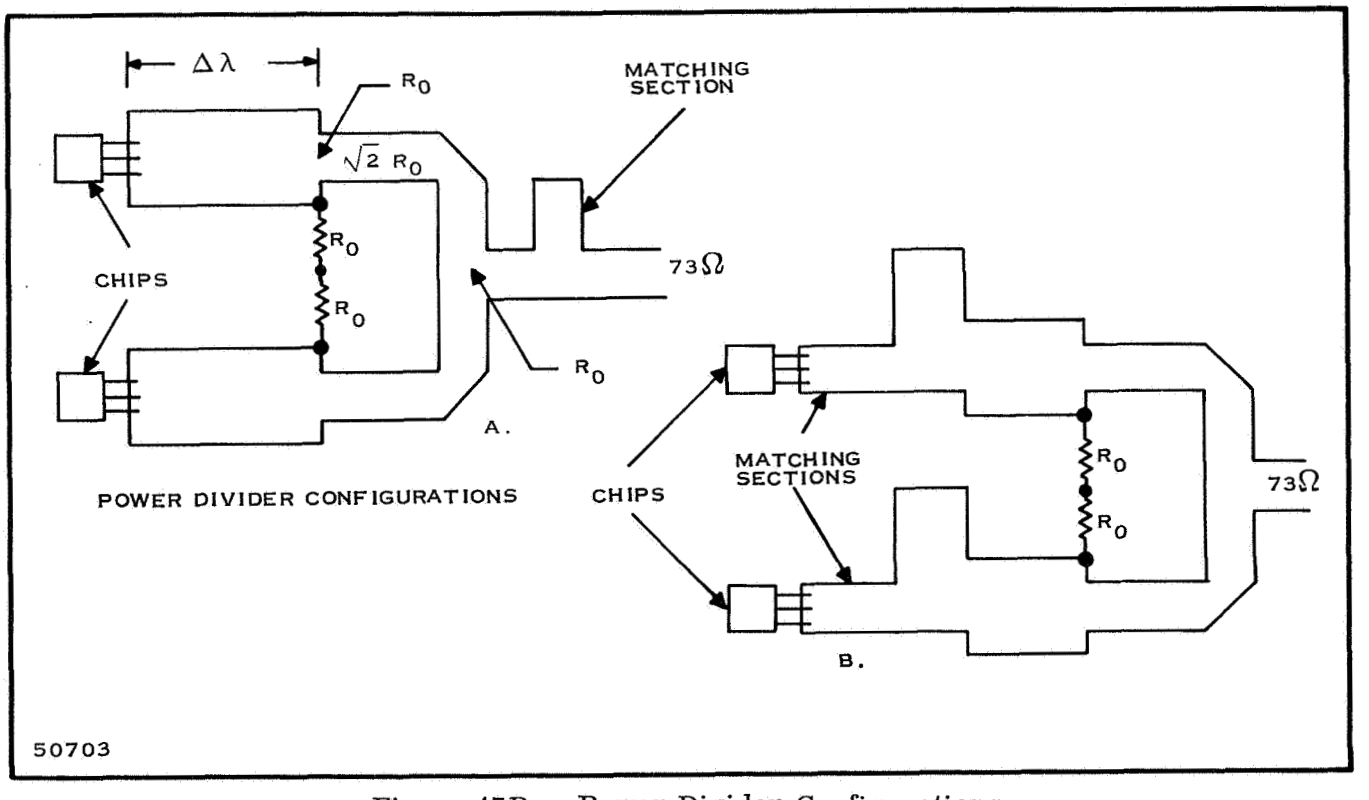


Figure 47B. Power Divider Configurations

Smith Chart is point 1 of Figure 48. The impedance is rotated toward the load along a circle of constant VSWR until it intersects the all real axis (point 2 of Figure 48). At this point Y_{out} is $(0.125 + j0)\ 20 \times 10^{-3}$ mhos, or, in terms of resistance, 400 ohms. Since the characteristic impedances of transmission lines on a 20-mil glazed ceramic substrate are limited to values between 20 and 120 ohms, the 400-ohm impedance of the divider is prohibitive. If point 2 of Figure 48 is rotated an additional quarter wave length toward the load, point 3 is reached. The admittance Y_{out} at point 3 is $(8 + j0)$ 20×10^{-3} mhos, which corresponds to a resistance of 6.25 ohms (an unusable line impedance for a 20-mil glazed ceramic substrate). Therefore, the configuration of Figure 47A will be discarded and that of Figure 47B will be used.

In Figure 47B the output impedance will be set to 73 ohms, all resistive. Using this valve for R_0 and the diagram of Figure 46, the impedance levels in the divider can now be determined.

$$R_0 = 73 \text{ ohms}$$

$$2\ R_0 = 103 \text{ ohms}$$

For the complete power divider configuration a matching section is used at each input port to match the transistor chip output impedance to the input of the power divider. The final output power divider configuration, with the matching sections, is shown in Figure 49.

The physical size of the power divider network on 1/16-inch Teflon-filled fiberglass printed circuit board is shown in Figure 50. The isolation resistors will be combined into one 146-ohm resistor.

The input power divider will split the power out of the L-158C Class A amplifier and drive two L-158C devices, operating Class C.

The dynamic admittances of these amplifiers are shown below.

Frequency	Class A Y_o^* (mmhos)	Class C Y_{in}^* (mmhos)
2.20 GHz	1.8 + j8.2	27.0 - j58.0
2.25	1.8 + j8.2	39.0 - j46.0
2.30	2.0 + j8.4	29.0 - j52.2

The variation of the real part of Y_{in}^* is too large to consider it constant [i.e., it varies from 27×10^{-3} mhos (37 ohms) to 39×10^{-3} mhos (26 ohms)], therefore, a matching section will be used at all three ports on the power divider.

Since the characteristic impedance of the power divider needs to be established before the matching sections can be designed, it will be determined first. With the characteristic impedance of the divider equal to the geometric mean of the real part of the two impedances to be matched at midband

$$Z_0 = R_0 = 1/\sqrt{(Y_{or}^*)\ (Y_{inr}^*)}$$

$$R_0 = 1/\sqrt{(1.8)\ (39) \times 10^{-6}} = 119\ \Omega$$

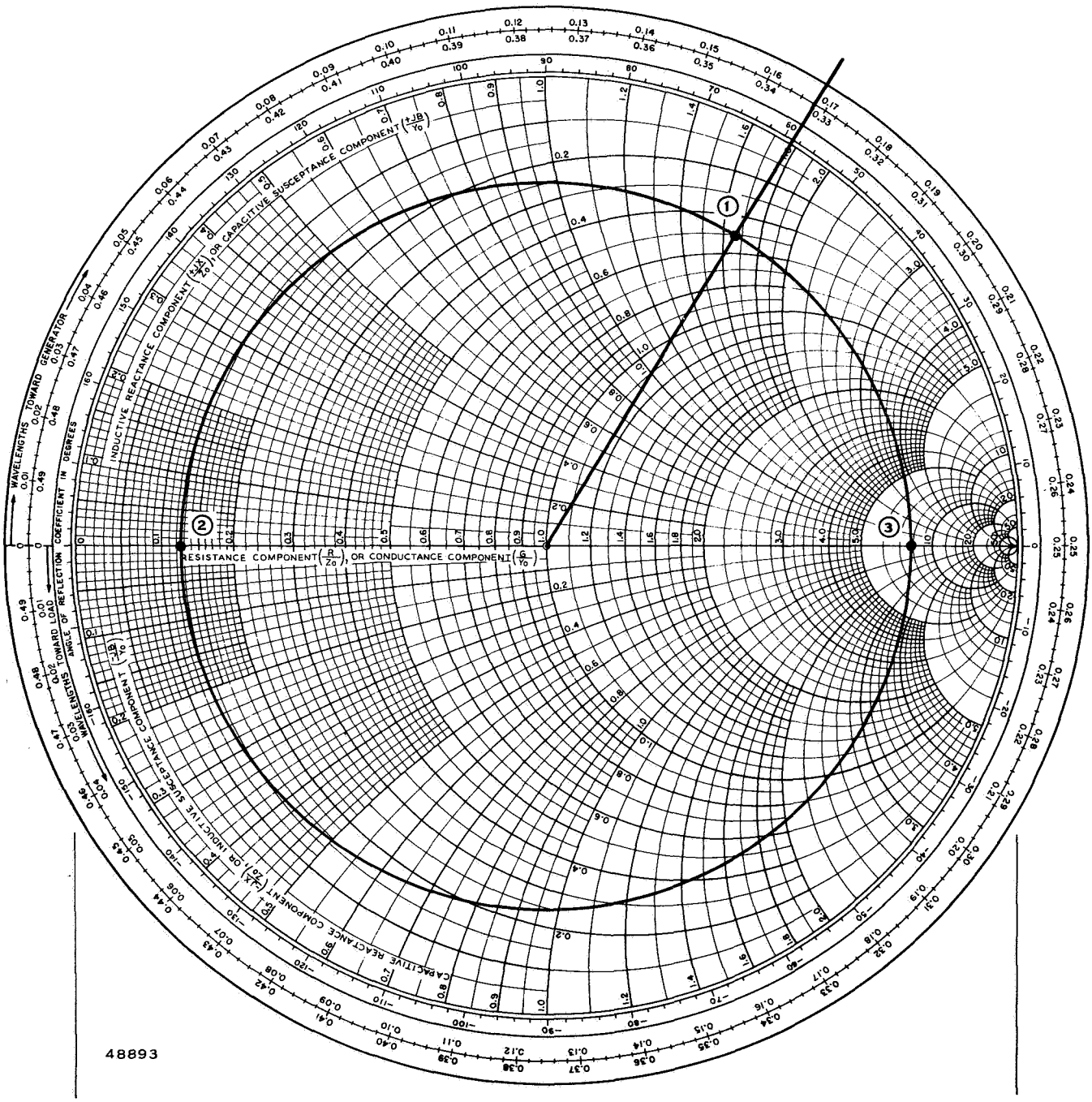


Figure 48. Sample Calculations

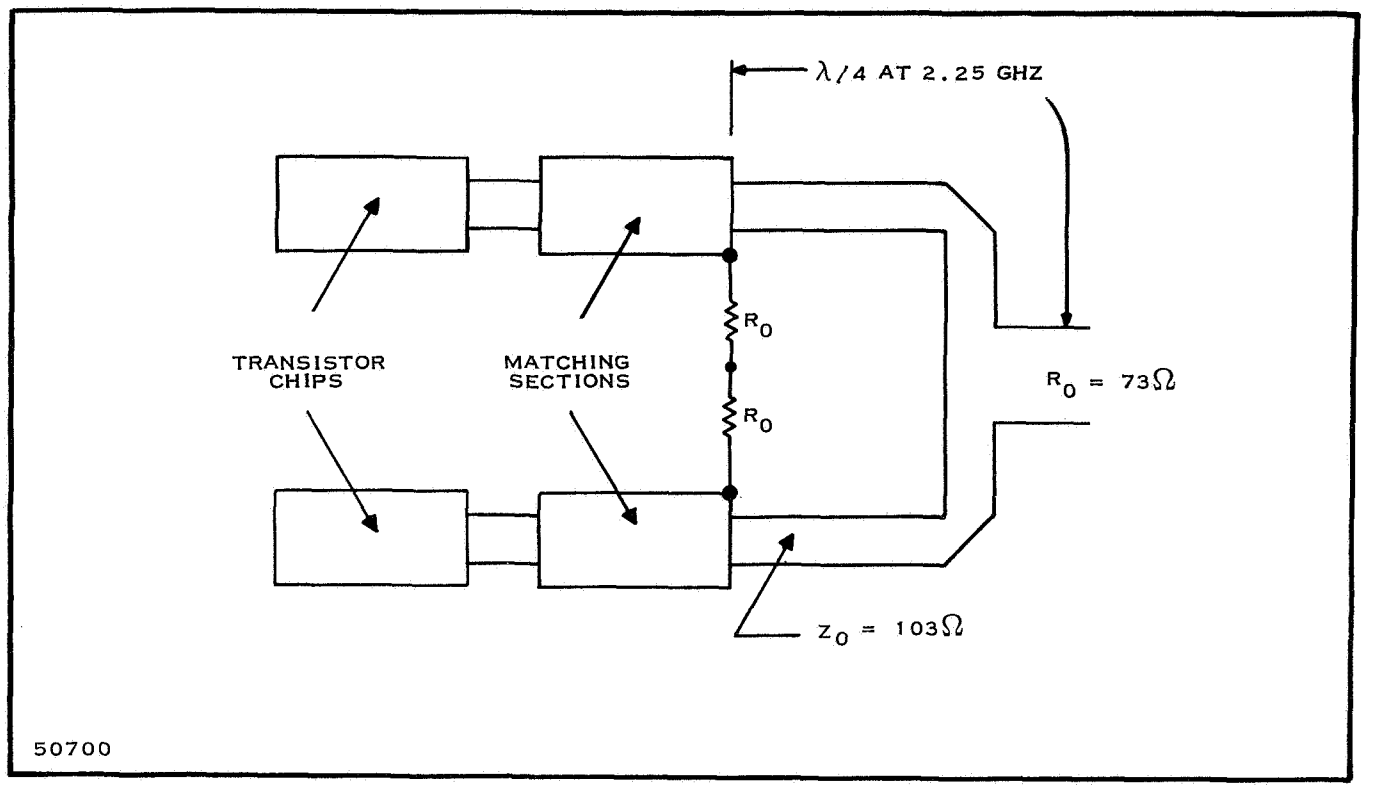


Figure 49. Power Divider Configuration

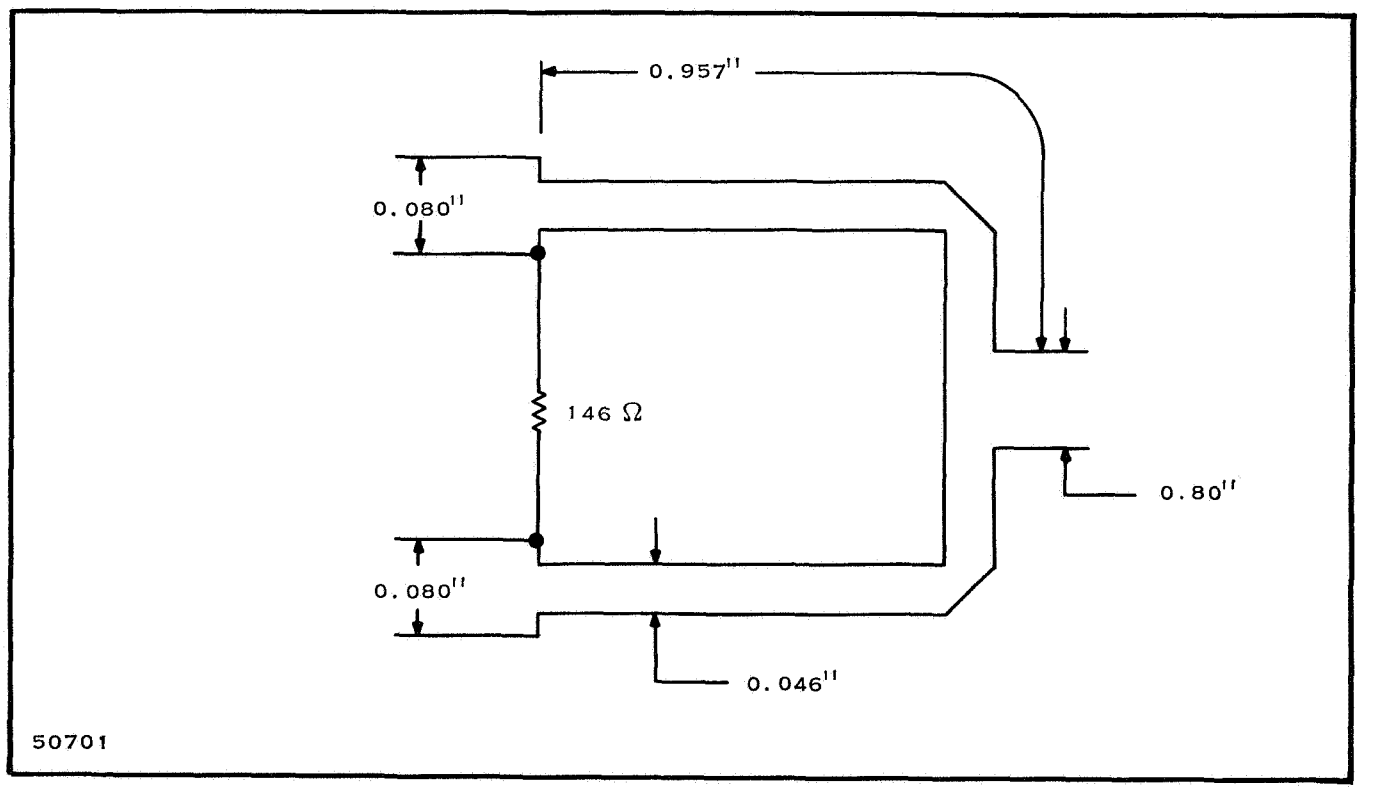


Figure 50. Teflon Board Layout

The impedance of the 1/4-wave transformer in the divider is

$$Z = \sqrt{2}\, R_o = 168\ \Omega$$

This level of impedance is prohibitive on 20-mil glazed ceramic. To simplify the design, since Z can take on any value from 120 ohms to 20 ohms, the impedance values used in the output power divider will also be used in the input power divider.

$$R_o = 73\ \Omega$$

$$Z = \sqrt{2}\, R_o = 103\ \Omega$$

Matching sections will be used at all three ports of the power divider to match the appropriate transistor admittances to the power divider.

Two of the power dividers previously described were built on 1/16-inch Teflon fiberglass board and tested (Figure 51). A 146-ohm 1/8-watt carbon composition resistor was used for the isolation resistor and a 60-ohm 1/4-wavelength matching section was used to match the 73-ohm inputs and outputs to 50 ohms.

As can be seen from table XII, the isolation between ports B and C is not good; this was caused by the isolation resistor being too long. The electrical length from the resistor and output transmission line junction to the common resistor tie point (the middle of the resistor, since only one resistor is used) should be a small portion of a wavelength or a multiple of 180 degrees. To improve the power divider performance a second divider was constructed, in which the electrical length from the resistor and output transmission line junction to the common tie point was made as small as physically possible. Test results from this divider are shown in table XIII, confirming the expected improvement in the isolation between ports B and C. The slight increase in the VSWR at port A probably is due to the 1/4-wavelength section at port A or because the microstrip to coax adapter was not optimized.

Table XII

Power Divider No. 1 Test Data

Frequency	VSWR Port A	VSWR Port B	VSWR Port C	Isolation Between Ports B and C	Insertion Loss Port C to A	Insertion Loss Port B to A
(GHz)				(dB)	(dB)	(dB)
2.20	1.16	1.38	1.34	11.2	0.14	0.25
2.25	1.13	1.37	1.32	11.6	0.22	0.36
2.30	1.09	1.27	1.28	12.0	0.17	0.35

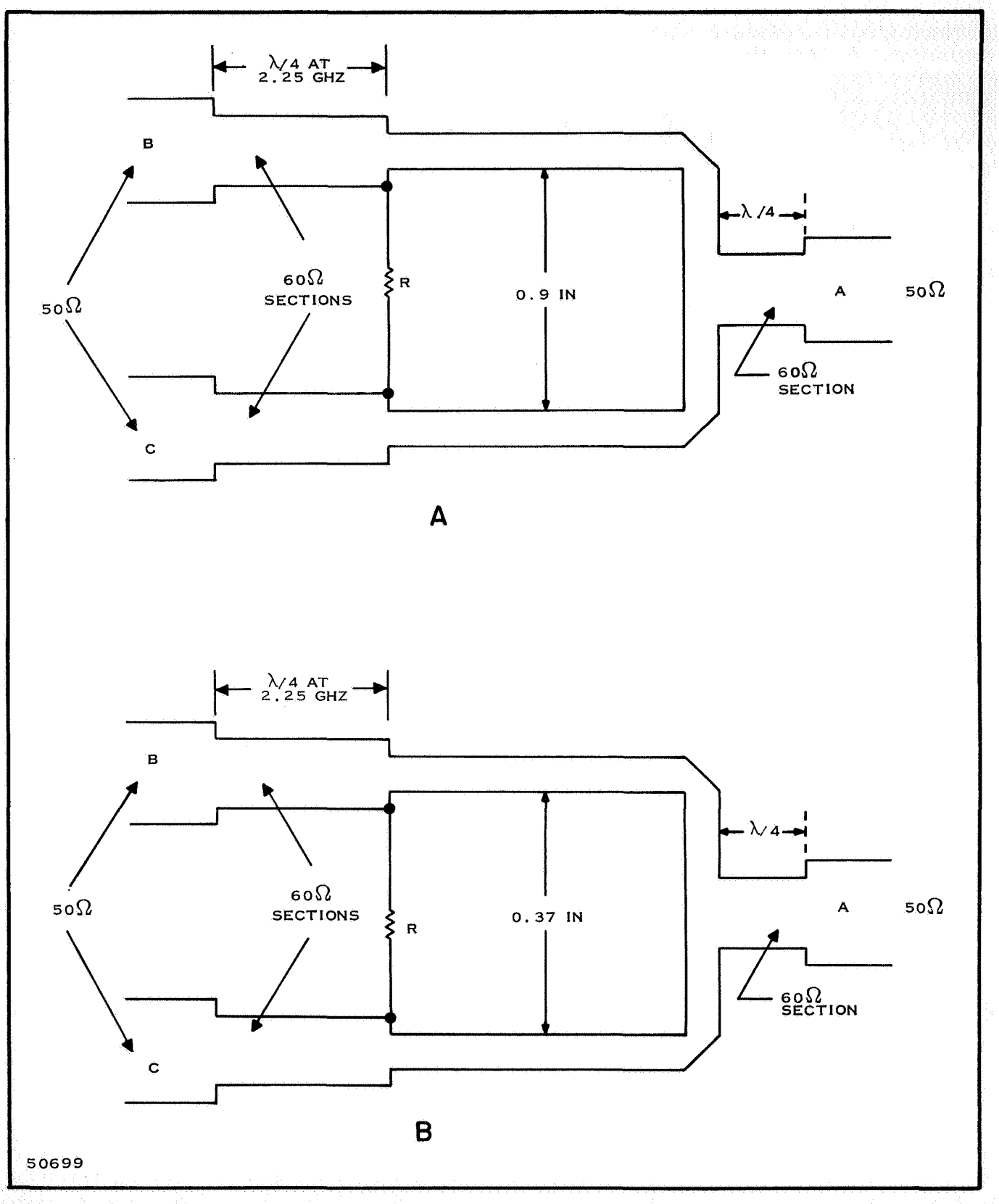


Figure 51. Power Divider

Table XIII

Power Divider No. 2 Test Data

Frequency	VSWR Port A	VSWR Port B	VSWR Port C	Isolation Between Ports B and C	Insertion Loss Port C to A	Insertion Loss Port B to A
(GHz)				(dB)	(dB)	(dB)
2.20	1.33	1.31	1.28	21.6	0.2	0.2
2.25	1.28	1.30	1.27	23.2	0.2	0.1
2.30	1.25	1.27	1.26	25.1	0.2	0.2

4. Impedance Matching Networks

Having determined the dynamic input and output admittances of the devices and the characteristic impedance of the power divider, the interstage and output matching networks can be designed. The design of these matching networks has been optimized by the use of a computer program, results of which are shown in Figures 52 through 56. A complete layout is shown in Figure 57, incorporating all of the matching sections and both power dividers. The physical location of the elements as shown in Figure 57 is only one of many possible arrangements.

5. Ceramic Design

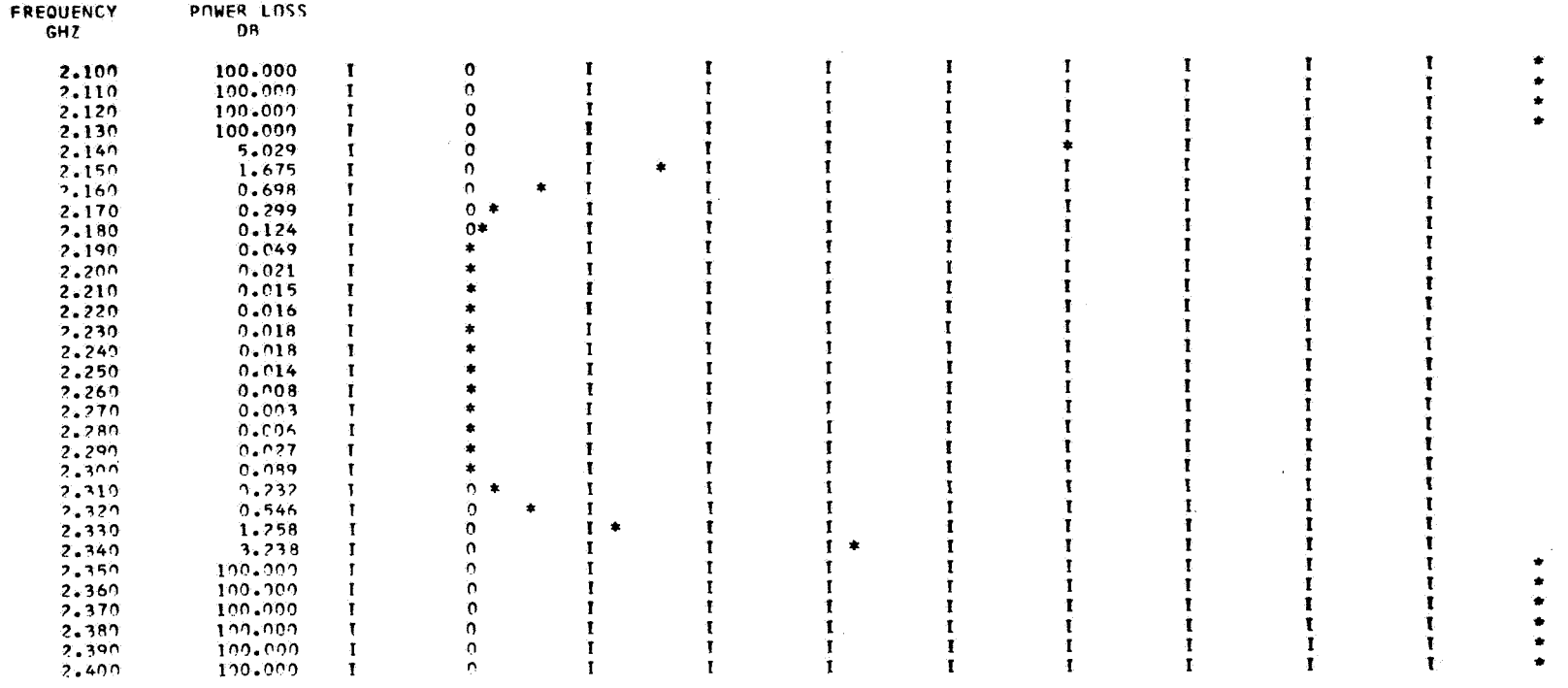
At the present time ceramic test circuits are being fabricated for use in testing the dissipation characteristics of the L-158A devices. The test circuits will also serve as a means of characterizing the chip transistor without the presence of package parasitics. The chip devices will be mounted on the test circuit exactly as they will be on the final thin-film circuit.

A layout of the ceramic test circuit is shown in Figure 58. The ceramic is 20 mils thick. In order to improve the heat flow away from the device, a 1/4-inch stud is bonded to the ground plane side of the test circuit (Figure 59). The stud is threaded, to allow clamping of the stud and ground plane to a test stand.

Special microstrip to coax adapters have been designed to facilitate testing of the ceramic breadboards. These adapters have proven to be extremely good electrically (VSWR's typically of 1.06) and are easily manipulated. The entire ceramic test setup is shown in Figure 60.

C. Multiplier Output Bandpass Filter

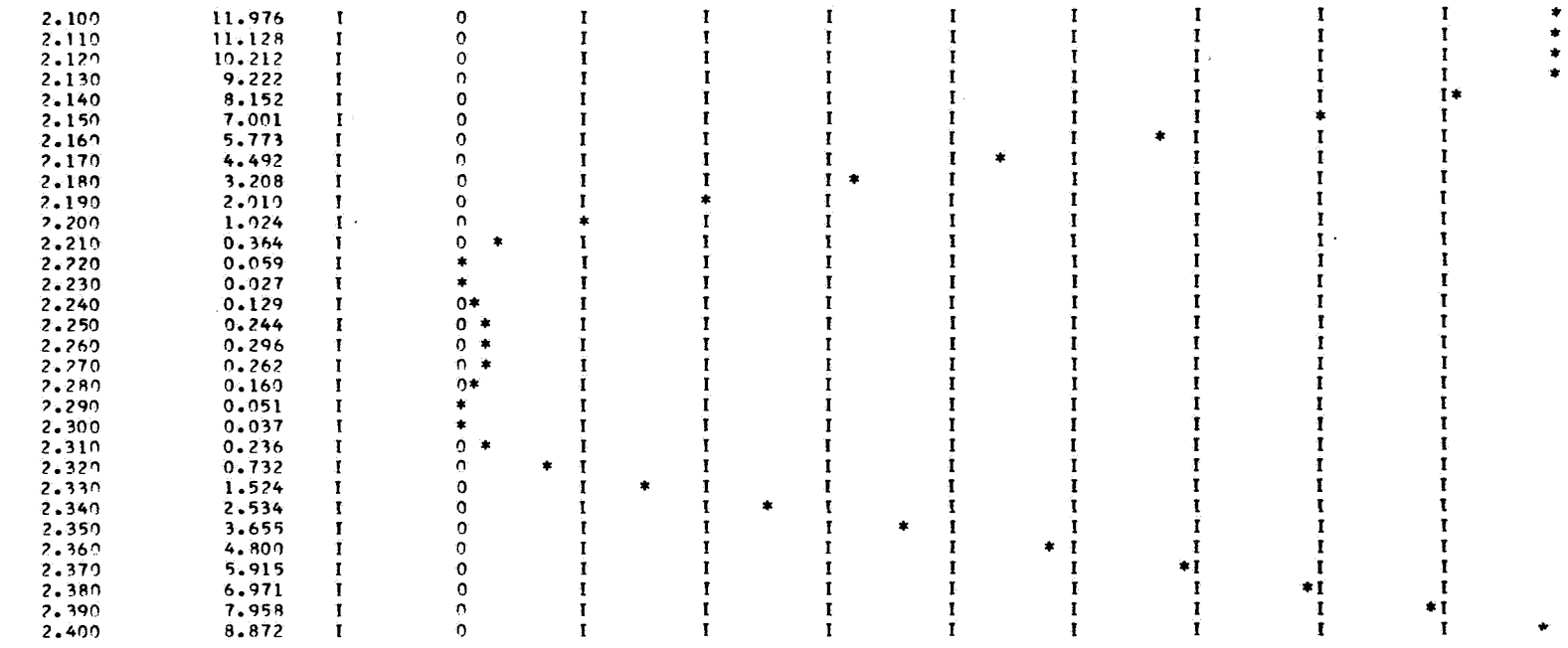
During the report period the multiplier output bandpass filter design employing microstrip techniques was developed, utilizing the main parts of a program written at Texas Instruments, Optimal Design of Matching Networks for Microwave Transistor Amplifiers.



ELEMENT	TYPE	WIDTH	LENGTH
1	FAT SERIES SECTION	64.1	682.2
2	OPEN STUB	355.4	347.4
3	GENERAL SERIES SECTION	355.4	205.0

Figure 52. Matching Network Response (50 Ohms to Input of L-158C, Class A)

FREQUENCY GHZ	POWER LOSS DB
2.100	11.976
2.110	11.128
2.120	10.212
2.130	9.222
2.140	8.152
2.150	7.001
2.160	5.773
2.170	4.492
2.180	3.208
2.190	2.010
2.200	1.024
2.210	0.364
2.220	0.059
2.230	0.027
2.240	0.129
2.250	0.244
2.260	0.296
2.270	0.262
2.280	0.160
2.290	0.051
2.300	0.037
2.310	0.236
2.320	0.732
2.330	1.524
2.340	2.534
2.350	3.655
2.360	4.800
2.370	5.915
2.380	6.971
2.390	7.958
2.400	8.872



ELEMENT	TYPE	WIDTH	LENGTH
1	GENERAL SERIES SECTION	299.1	192.4
2	FAT SERIES SECTION	49.5	653.4
3	SHORTED STUB	82.7	336.2
4	GENERAL SERIES SECTION	79.4	354.1

Figure 53. Matching Network Response (Output of L-158C to Input of Power Divider)

FREQUENCY GHZ	POWER LOSS DB
2.100	1.487
2.110	1.246
2.120	1.022
2.130	0.816
2.140	0.632
2.150	0.472
2.160	0.338
2.170	0.230
2.180	0.149
2.190	0.091
2.200	0.055
2.210	0.034
2.220	0.025
2.230	0.021
2.240	0.019
2.250	0.016
2.260	0.013
2.270	0.013
2.280	0.018
2.290	0.033
2.300	0.061
2.310	0.105
2.320	0.164
2.330	0.239
2.340	0.328
2.350	0.430
2.360	0.542
2.370	0.662
2.380	0.788
2.390	0.919
2.400	1.051

ELEMENT	TYPE	WIDTH	LENGTH
1	FAT SERIES SECTION	49.9	282.5
2	OPEN STUB	355.4	495.7
3	GENERAL SERIES SECTION	355.4	194.2

Figure 54. Matching Network Response (Output of Power Divider to Input of L-158C, Class C)

FREQUENCY GHZ	POWER LOSS DB
2.100	100.000
2.110	100.000
2.120	100.000
2.130	100.000
2.140	100.000
2.150	100.000
2.160	7.011
2.170	2.912
2.180	1.281
2.190	0.527
2.200	0.190
2.210	0.059
2.220	0.024
2.230	0.027
2.240	0.037
2.250	0.044
2.260	0.044
2.270	0.043
2.280	0.050
2.290	0.080
2.300	0.151
2.310	0.289
2.320	0.531
2.330	0.930
2.340	1.576
2.350	2.637
2.360	4.524
2.370	9.018
2.380	100.000
2.390	100.000
2.400	100.000

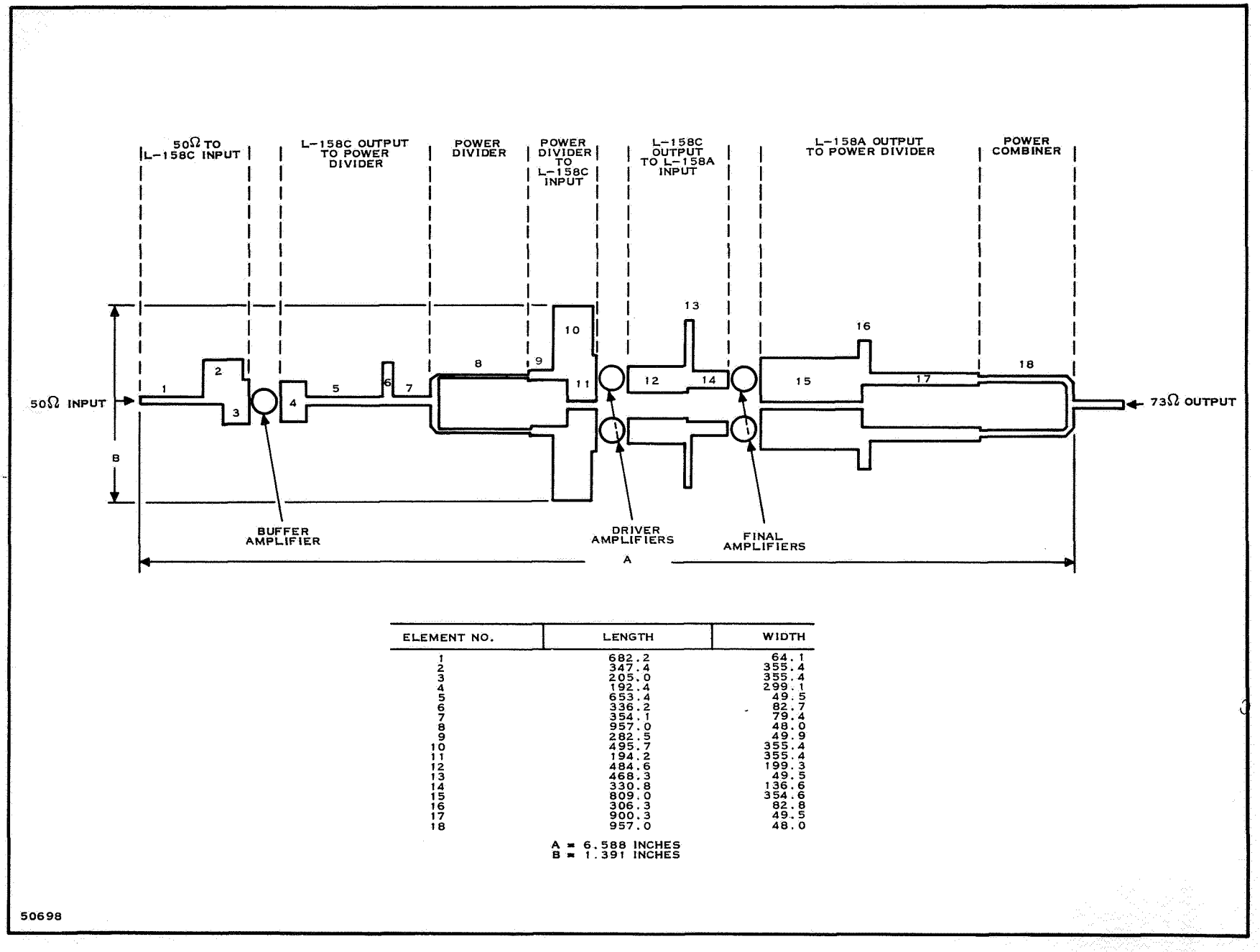
ELEMENT	TYPE	WIDTH	LENGTH
1	FAT SERIES SECTION	199.3	484.6
2	OPEN STUB	49.5	468.3
3	GENERAL SERIES SECTION	136.6	330.8

Figure 55. Matching Network Response (Output of L-158C to Input of L-158A)

FREQUENCY GHZ	POWER LOSS DB
2.100	100.000
2.110	100.000
2.120	15.631
2.130	4.842
2.140	2.541
2.150	1.432
2.160	0.820
2.170	0.465
2.180	0.256
2.190	0.134
2.200	0.064
2.210	0.027
2.220	0.008
2.230	0.001
2.240	0.001
2.250	0.003
2.260	0.006
2.270	0.009
2.280	0.012
2.290	0.016
2.300	0.020
2.310	0.025
2.320	0.035
2.330	0.049
2.340	0.073
2.350	0.108
2.360	0.160
2.370	0.236
2.380	0.344
2.390	0.497
2.400	0.714

ELEMENT	TYPE	WIDTH	LENGTH
1	FAT SERIES SECTION	354.6	809.0
2	SHORTED STUB	82.8	306.3
3	GENERAL SERIES SECTION	49.5	900.3

Figure 56. Matching Network Response (L-158A Output to Input of Power Divider)



ELEMENT NO.	LENGTH	WIDTH
1	682.2	64.1
2	347.4	355.4
3	205.0	355.4
4	192.4	299.1
5	653.4	49.5
6	336.2	82.7
7	354.1	79.4
8	957.0	48.0
9	282.5	49.9
10	495.7	355.4
11	194.2	355.4
12	484.6	199.3
13	468.3	49.5
14	330.8	136.6
15	809.0	354.6
16	306.3	82.8
17	900.3	49.5
18	957.0	48.0

A = 6.588 INCHES
B = 1.391 INCHES

50698

Figure 57. Power Amplifier Layout

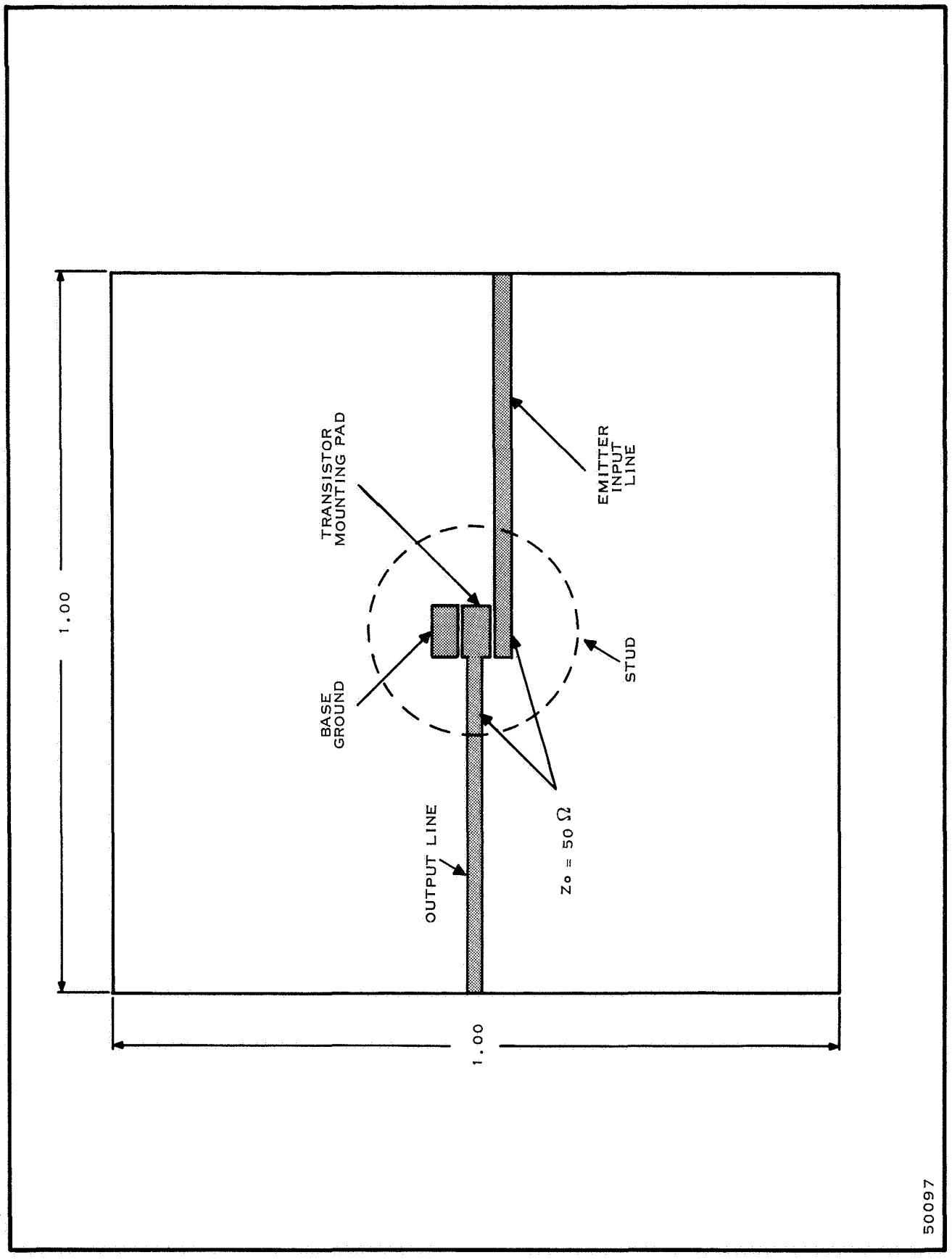


Figure 58. Ceramic Test Circuit

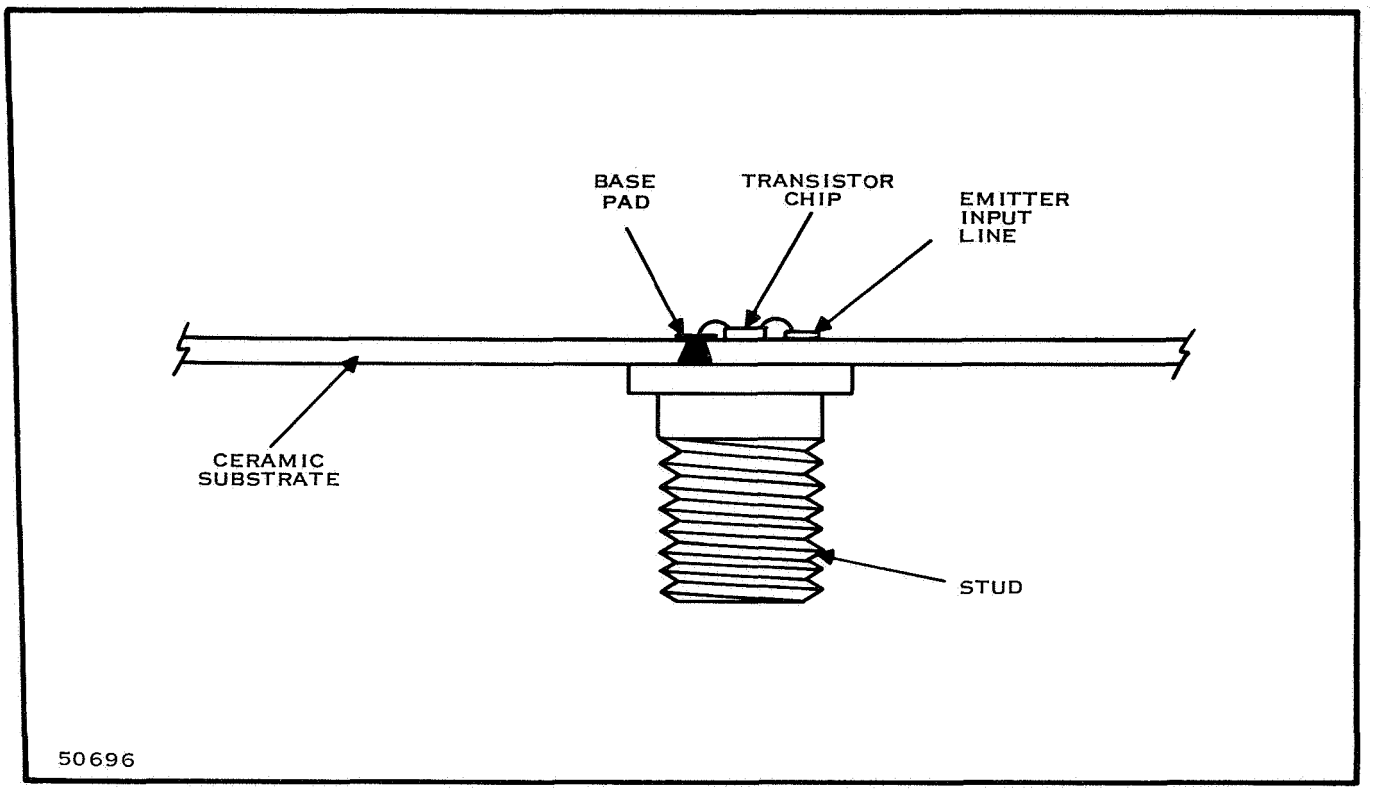


Figure 59. Ceramic Test Circuit and Stud

The program consists of the same basic parts as the previously mentioned program, except that the elemental values were adjusted to fit the filter response to a desired response. The new input includes upper and lower limits on the passband and the desired response curve. This response curve is specified at a set of frequencies in a certain range along with the power loss desired at each frequency. At any stage in the curve fitting process, how well the curve matches the desired curve is determined by means of the value of a "merit function", which is the sum of the magnitudes of the difference in the power loss between the curve and the desired curve. The purpose of the program is to minimize the merit function.

The present program was used to obtain a bandpass characteristic that approaches the curve of Figure 61. The response is flat in the band (2.2 to 2.3 GHz) and drops at some rate until it is 40 dB at 1.8 and 2.7 GHz. This "merit function" is the goal for the filter design.

The results of the program have yielded a 9-element filter (5 series elements, 4 shunt elements) which approaches the design goals. The final filter response (shown in Figure 62) resulted in a mid-band insertion loss of 0.375 dB; the attenuation increases rapidly to 22.54 dB at 2.7 GHz and 29.95 dB at 1.8 GHz. Although this attenuation is not as great as desired, it was considered optimum for a 9-element filter. Increasing the number of elements would make the size of the filter unreasonable.

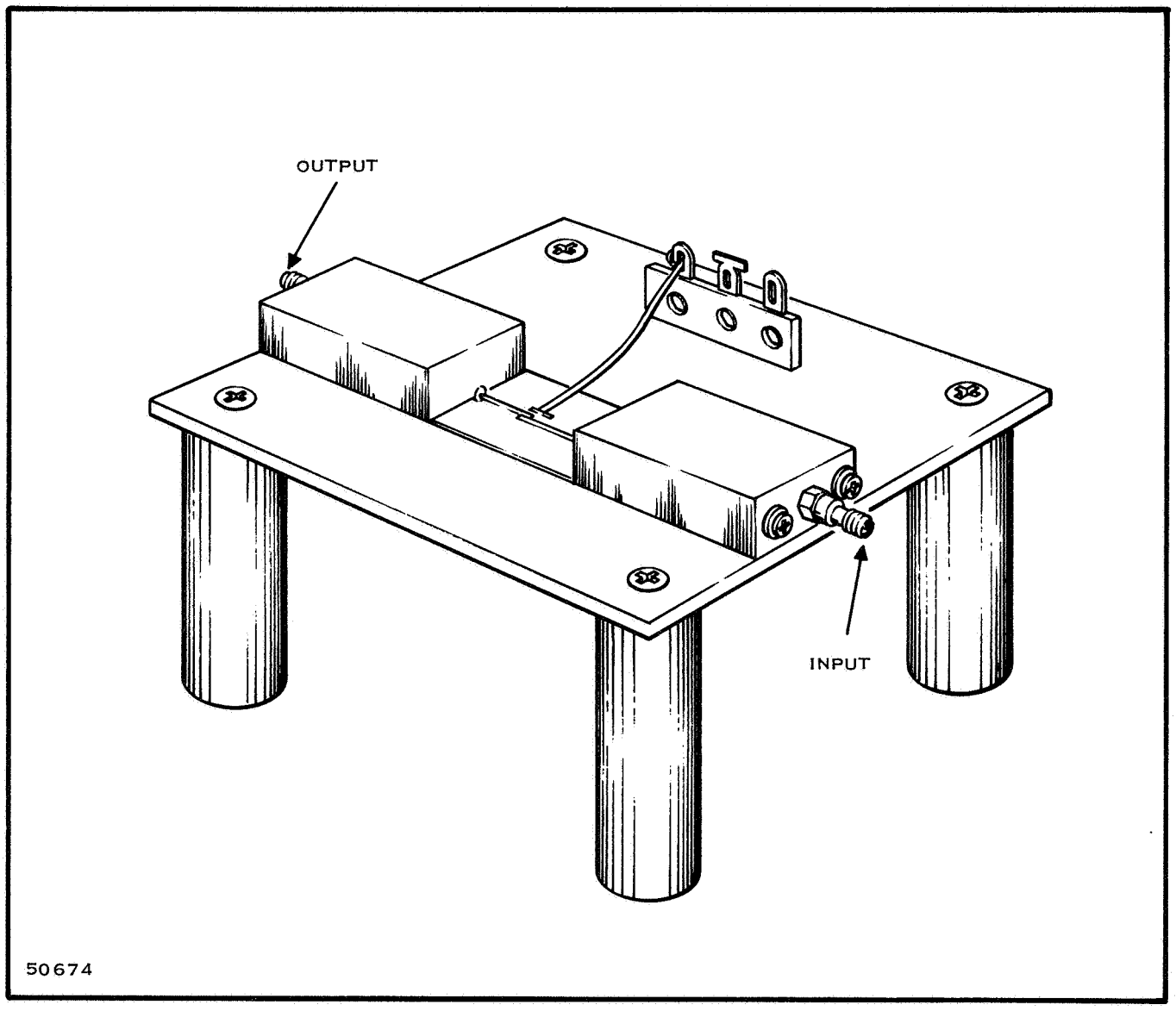


Figure 60. Ceramic Test Setup

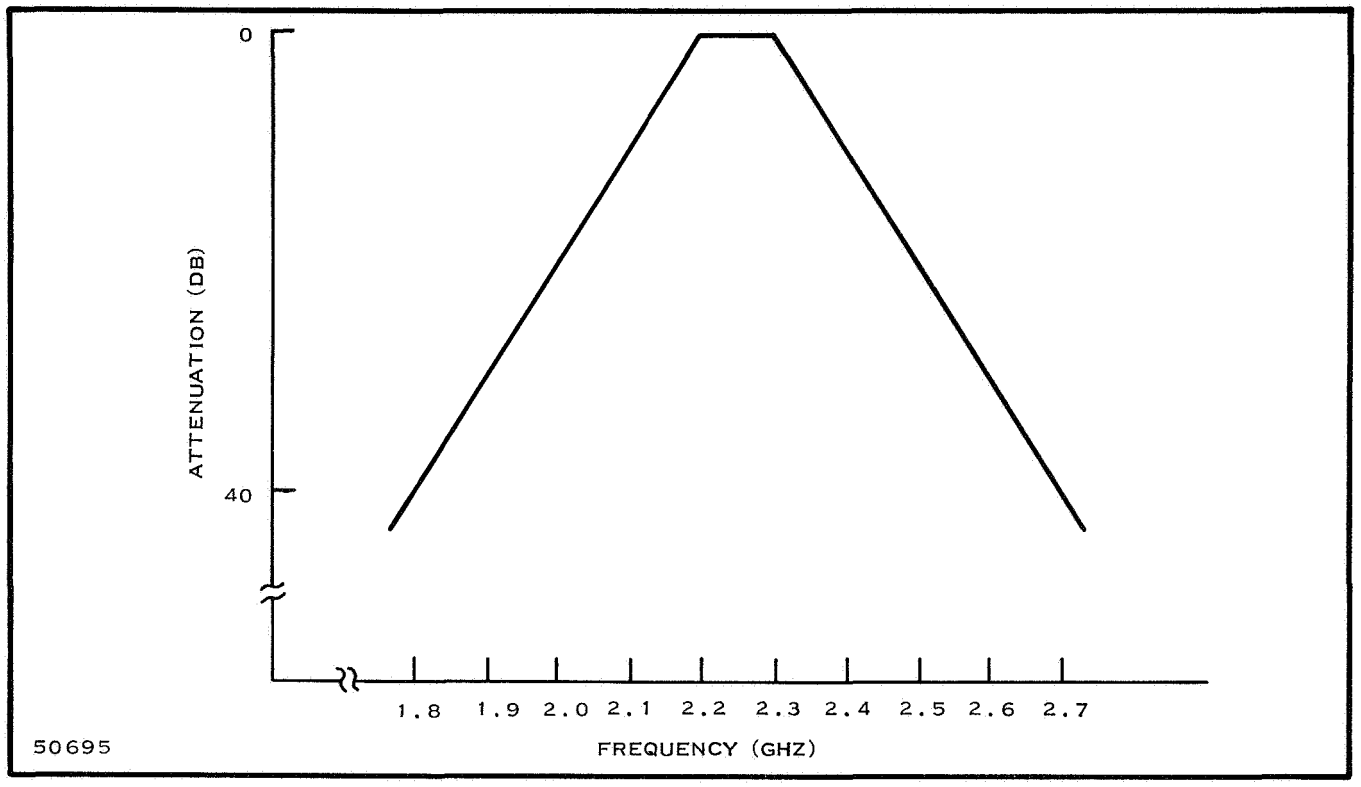


Figure 61. Bandpass Filter Response

The final individual element sizes are shown below for a 20-mil unglazed ceramic substrate.

ELEMENT	WIDTH (MILS)	LENGTH (MILS)
1. Series - Thin	3.7	550.8
2. Shorted Stub	154.4	410.2
3. Series - General	5.0	550.6
4. Shorted Stub	154.4	182.9
5. Series - General	41.8	504.7
6. Shorted Stub	120.7	380.4
7. Series - Thin	4.2	549.4
8. Shorted Stub	22.3	235.4
9. Series - General	35.8	519.4

The layout of the filter Figure 63 utilizes parallel shunt stubs to yield the low impedance elements required. The actual size of the filter is 600 mils by 935 mils and probably could be reduced if the elements were meandered more. However, to minimize coupling between elements, meandering was kept to a minimum.

Appendix A contains a detailed description of the program, including the Fortran Source Statement.

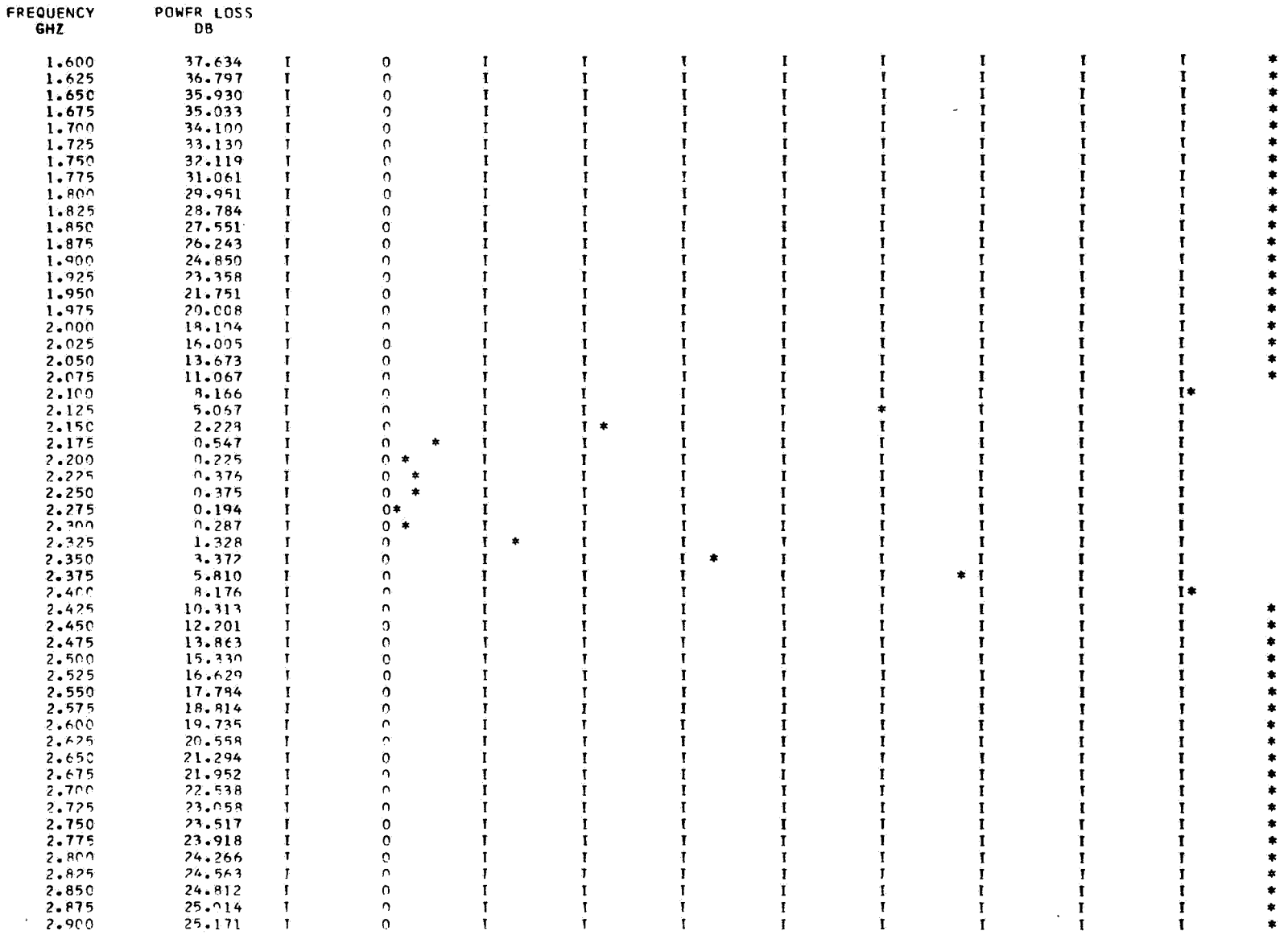


Figure 62. Bandpass Filter Response

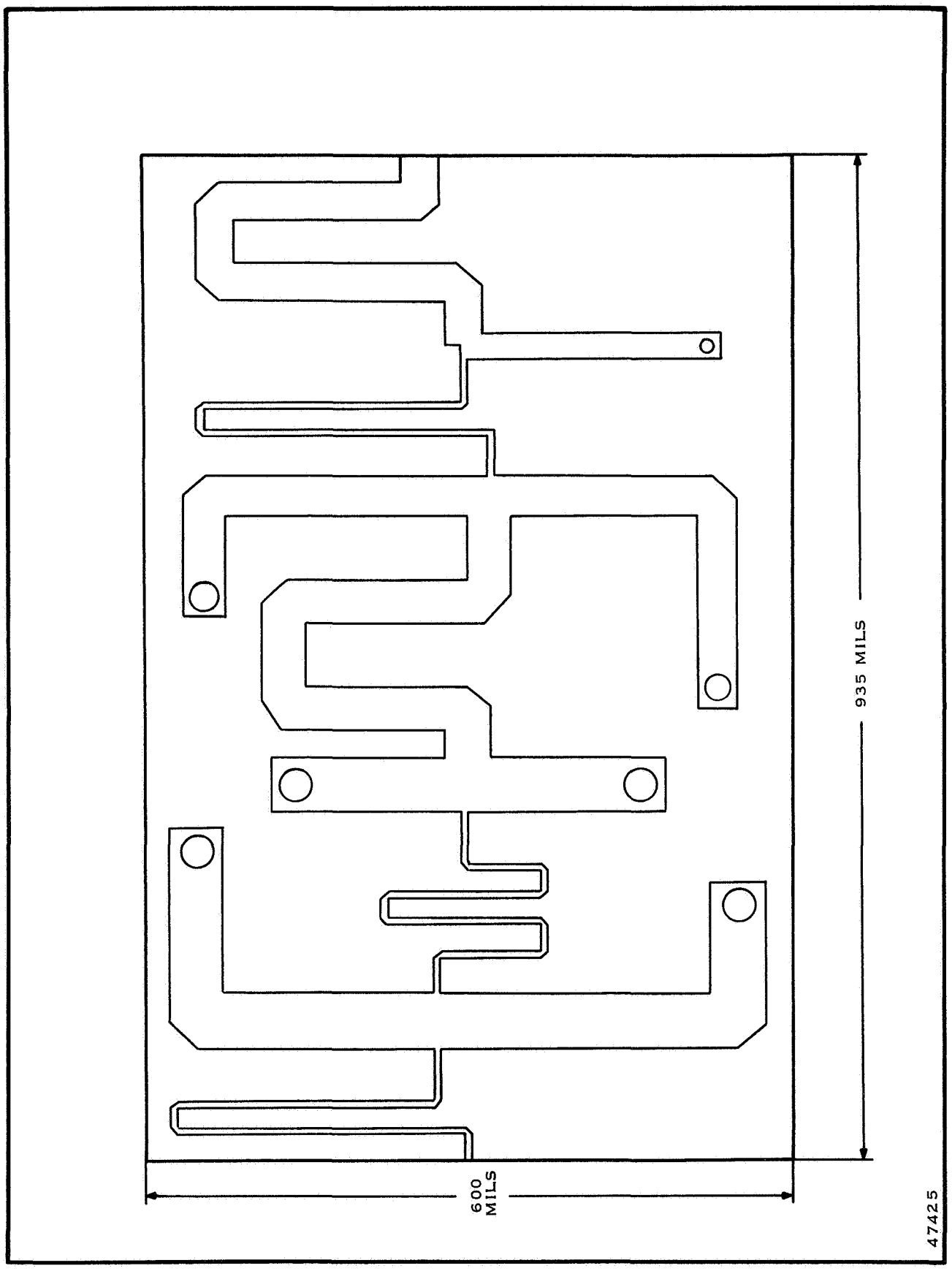


Figure 63. Reference Generator Output Filter

SECTION V

THERMAL INVESTIGATION

Since the power dissipation characteristics of the L-158A and L-158C devices are not known for CW operation, it appears at this point that an investigation of these characteristics is warranted. The importance of such an investigation is twofold: first, the actual dissipation limits of the devices could be determined under operating conditions (and compared against theoretical calculations for validity; second, the optimum physical location of the devices with respect to each other and the transmitter housing could be determined in order to insure thermal stability through proper packaging techniques.

With the use of an infrared microradiometer, the transistor junction operating temperature can be measured. From this the true thermal impedance of a device can be determined. In general, isothermal contour maps are constructed from consecutive IR profiles which illustrate the size and intensity of hot spots. The general thermal characteristics of a device can be studied by constructing such isothermal maps at different operating conditions.

The infrared microradiometer used in this type of study[9] consists basically of an InSb (Indium Antimony) photodetector that is sensitive to infrared radiation in the 2- to 5.6-μ range. Radiation is collected from a 1.5-mil-square spot and focused on the detector by a 15X Beck reflective objective lens. Amplification is achieved by mechanically chopping the radiation below the objective and using a phase-sensitive ac amplifier. A reference chamber is provided into which the detector looks when the mirrored chopper blade is interrupting the source radiation. The detector and the reference chambers are maintained at 77°K by liquid N_2 dewars. This instrument has a sensitivity of 0.5°K and an absolute accuracy of 1.0°K at 300°K for a blackbody. Subjects are mounted on an X-Y stage which has an automatic X drive with a manual Y adjustment. A position signal is obtained from a multiturn potentiometer connected to the drive mechanism. Infrared profiles are obtained by recording the amplifier output (infrared signal) versus the position signal on an X-Y recorder and on digital paper punch tape.

In order to convert the output signal of the instrument to actual temperature, the emissivity of the device surface must be known at every point. This poses a serious problem when the surface temperature of a semiconductor device must be determined. Generally, the emissivity varies on the surface from less than 0.05 on the metal contact areas to an apparent value of 0.6 to 0.8 on the silicon or oxide. The silicon actually is not opaque to radiation in the 2- to 5.6-μ region, so that part of the radiation signal originates from within the device. This situation not only distorts the thermal picture but introduces unknown variations which preclude quantitative measurement of surface temperature. It is essential, therefore, that some method of controlling surface emissivity be used.

This control is accomplished by coating the surface of the device with substances which provide uniform high-emissivity. The particular coating to be used is dependent upon the temperature range to be investigated and the information desired - temperature profiles or contour maps.

Figure 64 shows a temperature profile plot with excellent correlation between experimental and theoretical results.

Figures 65 and 66 are contour maps of a transistor before and after lateral thermal stability, respectively.

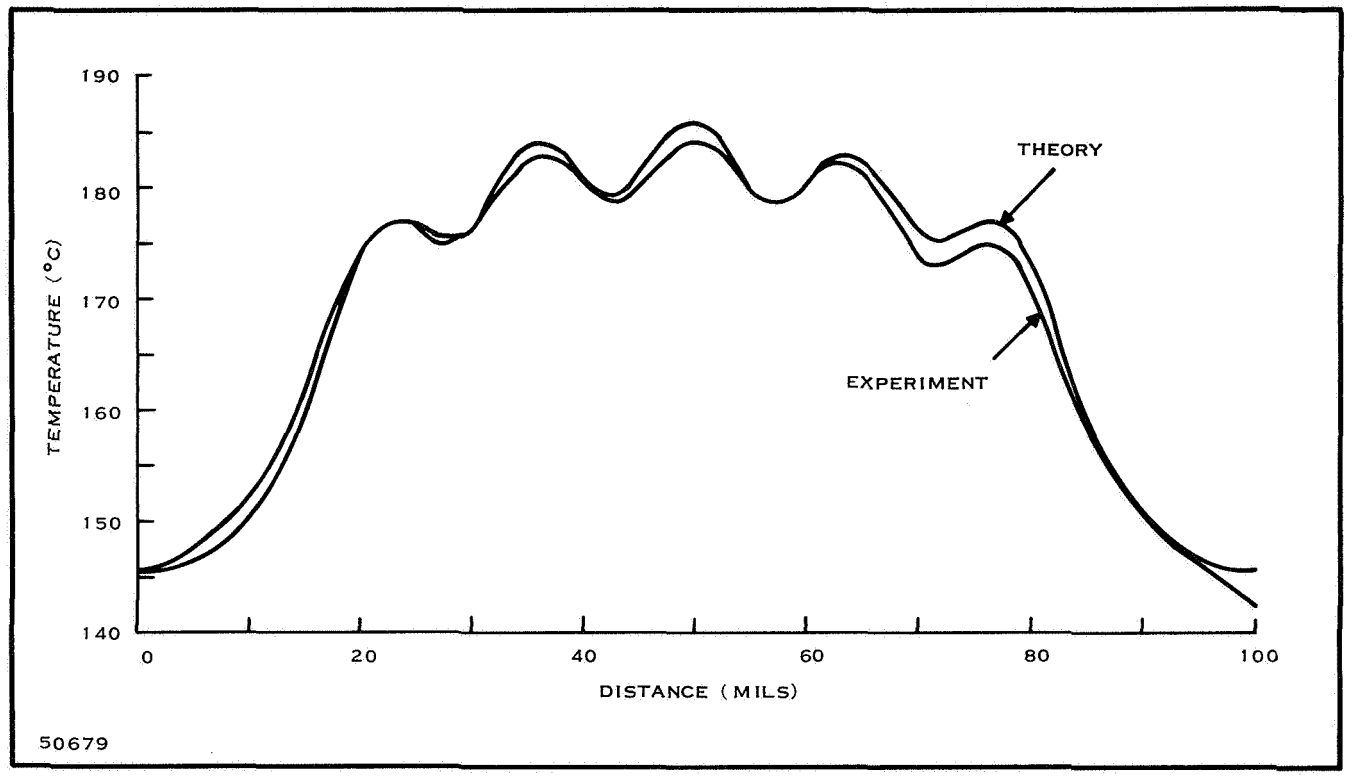


Figure 64. Comparison of Theoretical and Experimental Surface Temperature Profiles with Uniform Current Distribution

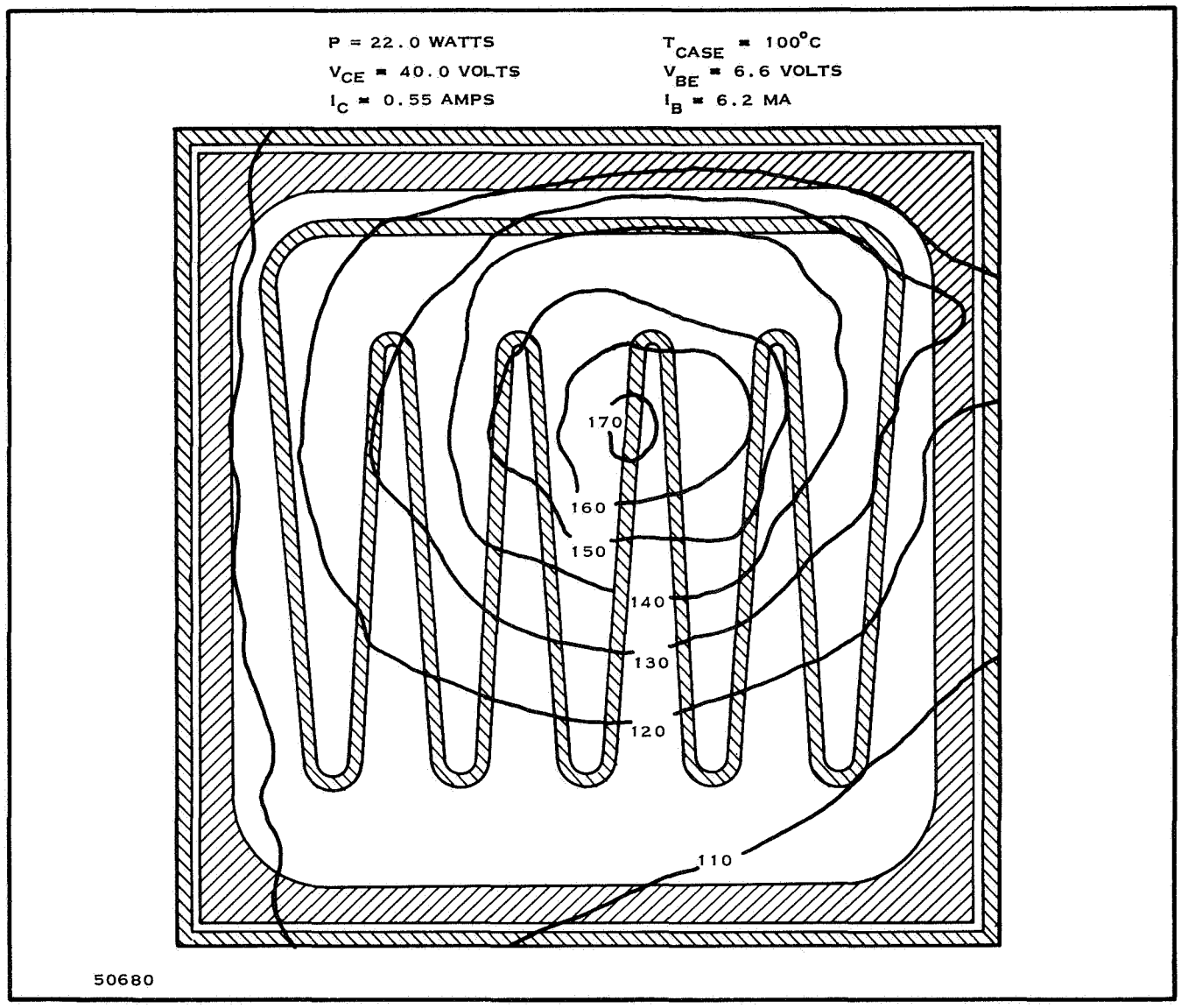


Figure 65. Isothermal Contour Map of a Transistor Before Lateral Thermal Instability

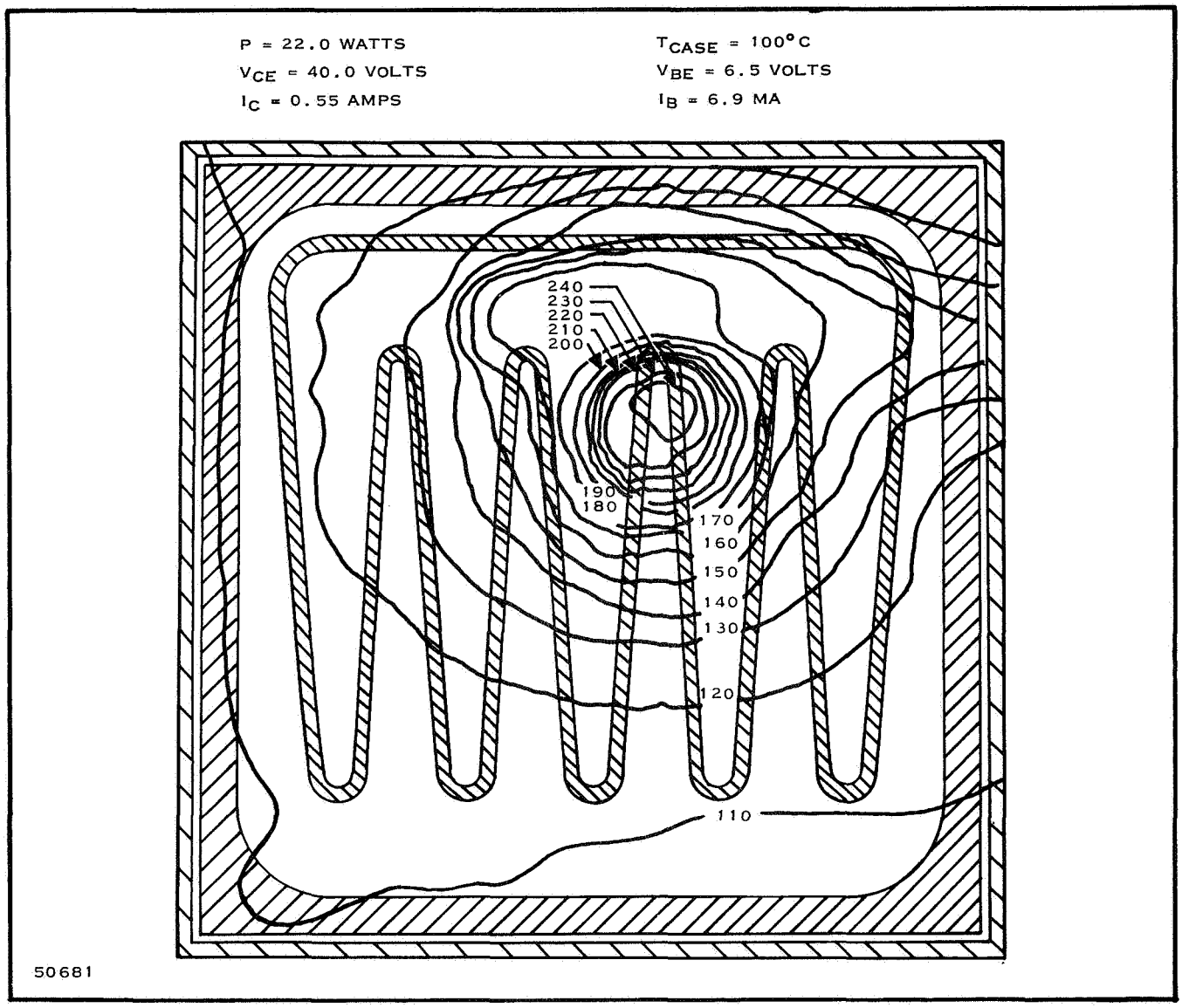


Figure 66. Isothermal Contour Map of a Transistor After Lateral Thermal Instability

SECTION VI

CONCLUSION

The next phase of the study will be devoted to fabrication and test of the breadboard VCO and power amplifier circuits and the fabrication of these circuits in thin-film hybrid form.

Further consideration will be given to the layout, arrangement and fabrication of the complete transmitter in monolithic or thin-film hybrid form to minimize size, weight, spurious radiation and interconnections.

The complete transmitter will be subjected to the test plan submitted in Phase IV to evaluate its performance as a system. Since many of the tests performed under the test plan do not have any definite requirements or specifications as a basis, the results of these investigative tests, along with the general specifications to which the transmitter was designed, could be used as a basis for future specifications applied to solid-state integrated microwave transmitters.

SECTION VII

PROGRAM PERSONNEL

Ben S. Skinner, Jr.	Project Engineer
Louis I. Farber	Senior Engineer
James C. Pinac	Engineer
Wayne J. Harrison	Technician

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APPENDIX A

FILTER PROGRAM

APPENDIX A

FILTER PROGRAM

Using an existing computer program for the design of matching microwave networks, several changes were made to ensure that the network so designed also had a bandpass characteristic. The original program, written by Frank Emery and Michael O'Hagen was discussed in Scientific Report No. 3.

A. ORIGINAL PROGRAM

With the input and output admittances specified at a given set of frequencies, the input admittance function and the output admittance function are generated by fitting these data to a second-degree polynomial in a least squares sense. These two admittance versus frequency functions, in turn, are used to specify the desired input or output admittance at any frequency. The topology of the network, i.e., the type of sections to be used, is then described and the characteristic admittances and electrical lengths are used as the variables in the merit function. The merit function is a measure of the goodness of the fit; an ideal design is one having a merit function value of zero. The merit function is then minimized by means of a pattern search routine. When a minimum is found, the characteristic admittances and electrical lengths of the section are printed and an on-line digital plot of the final response is made.

The pattern search routine starts from an initial point and determines a successful direction by searching a fixed distance from the initial point in a number of random orthogonal directions. If a successful direction is found, i.e., a point is found at which the value of the merit function is less than the current minimum, a series of moves is made in this direction while increasing the increments. If no successful direction is found, the increments are reduced and the exploratory moves are repeated. In this way, the value of the merit function decreases until either the increments are cut below a specified minimum or the number of iterations taken is larger than a specified maximum.

B. CHANGES

Most of the changes made in the program are involved with defining a new merit function. In order to obtain a bandpass characteristic, the desired power gain in the band, and at certain frequencies outside the band, is specified. The program then varies the characteristic admittance and electrical length of each section in such a way as to minimize the deviations of the output characteristic from the desired output characteristic. The new merit function chosen is the sum of the absolute values of the differences between the gain and the desired gain at certain specified frequencies. In order to minimize loss in the passband, the number of frequencies at which the merit function is evaluated should be much greater inside the passband than outside the passband.

A particular bandpass characteristic is specified by the following data: the upper and lower frequency limits for the passband, the specific frequencies outside the passband at which the merit function is to be evaluated, the number of frequencies

inside the passband at which the merit function is to be evaluated, the desired gain in the passband, and the desired gain at the maximum and minimum frequencies outside the passband at which the merit function is to be evaluated. For frequencies between the lowest frequency outside the passband and the low end of the passband, or for frequencies between the high end of the passband and the highest frequency outside the passband, the variation of gain with frequency is assumed by the program to be linear; i.e., if the desired gain at 1.0 gigahertz is 40 dB and the desired gain at 2.0 gigahertz is 0 dB, then the desired gain at 1.25 gigahertz and 1.5 gigahertz will be set at 30 dB and 20 dB respectively.

Practical design considerations limit the magnitudes of the characteristic admittances and the electrical lengths of the sections. The starting point for the pattern search routine is specified by a number, between zero and one, which indicates the fraction of the internal length, starting at the lower limit, at which the initial point is to be taken. Thus, for a given variable, if XL is the lower bound, XU is the upper bound and XMULT is the fraction which determines the starting point, then, with the internal length DX equal to XU - XL, the starting point is given by XL + XMULT * DX. This fraction XMULT may be specified by the user, or the user may let the computer select it randomly. However it is determined, the value XMULT is the same for all variables.

C. INPUT DATA

The input data consists of eleven types of data cards and must be in the order given below:

1. NDATA, [RUN(I), I = 1,10] FORMAT (I5, 5X, 10A6)

   NDATA = the number of data cards of the next type.

   RUN(I) = an alphanumeric header that will be printed in the output.

2. FF(I), YINR(I), YINI(I), YOUTR(I), YOUTI(I) FORMAT (8E10.0)

   There are NDATA of these cards and each card contains: a frequency in gigahertz, FF; the input admittance real and imaginary parts, YINR and YINI; the output admittance real and imaginary parts, YOUTR, YOUTI.

3. ICUE(I), [TYPE (I,J), J = 1,7], XYL(I), XYU(I), XBL(I), XBU(I)

   FORMAT (I5,7A5, 4E10.0)

   There are seven of these cards, and each contains: The line section cue number, ICUE: an alphanumeric field containing the name of the section, TYPE (·,J); the lower and upper bounds on the characteristic admittance, XYL and XYU; the lower and upper bounds on the electrical length, XBL and XBU.

The line section cue numbers are defined as follows:

1. Fat Series Section
2. Thin Series Section
3. General Series Section
4. Shorted Stub
5. Open Stub
6. Shunt Capacitor, Y_o = C, BL = R
7. Series Capacitor, Y_o = C, BL = R

4. KMAX, KRMAX, ISW, INDEX, REDUCE, SPEED, SMOOTH, GROW, BL

FORMAT (415,6E10.0)

This card contains the data for the pattern search routine:

KMAX = The maximum number of iterations.

KRMAX = The number of successful steps taken before increasing the increments.

ISW = Detail print switch. If non-zero, values are printed each time a smaller value is found.

INDEX = The number of the variable on which minimal step tests are made.

REDUCE = The factor for decreasing step size on failure.

SPEED = The factor for increasing step size on success.

SMOOTH = Exponential smoothing factor for adjusting steps.

GROW = Exponential growth on successful steps.

BL = The minimum increment allowed. BL is tested only with the (INDEX) th variable.

5. NFQ, NFP, REFQ, FLOQ, FHIQ, FLOP, FHIP, SLOPE

FORMAT (2I5,7E10.0)

NFQ = The number of frequencies used in the evaluation of the merit function.

NFP = The number of frequencies used in the final digital plot.

REFQ = The reference frequency.

FLOQ, FHIQ = The low and high frequencies of the evaluation interval.

FLOP, FHIP = The low and high frequencies of the plot.

6. NFIN, NFOUT, FMIN, FMAX FORMAT (2I5, 2E10.0)

NFIN, NFOUT = The number of evaluation frequencies inside and outside the passband.

NFOUT must ben an even number.
(NFIN + NFOUT = NFQ)

FMIN, FMAX = The low and high frequencies of the passband.

7. FOUT(I), I = 1, NFOUT FORMAT (8E10.0)

These are the specific frequencies outside the passband at which the merit function is to be evaluated.

8. PT1, PT2, PT3 FORMAT (5F5.0)

PT1 = The desired gain at FLOQ.

PT2 = The desired gain in the passband.

PT3 = The desired gain at FHIQ.

(Gain is expressed in decibels.)

9. NNCUES, MORE, KCODE, NOROT, NTRL FORMAT (1615)

NNCUES = The number of filter elements.

MORE is a code for more data and will be explained below:

KCODE = The code for the line dimension.

NOROT = 0.

NTRL indicates how the starting point for the pattern search routine is to be chosen. If NTRL is zero, the starting point is determined by the number XMULT on the next card.

If NTRL is non-zero, the starting point is chosen randomly NTRL times. An optimum design is made for each of the NTRL starting points.

10. XMULT FORMAT (E10.0)

XMULT = The number to determine the starting point if NTRL is zero.

NOTE: If NTRL is non-zero, this data card must be in the data deck, even though the data on it will not be used.

11. NCUE(I), I = 1, NNCUES FORMAT (16I5)

This card describes the network topology.

NCUE(I) = The line section cue number of the I^{th} section.

The last three cards describe the initial network. If several networks with the same limits are to be optimized with one pass on the computer, it is only necessary to make up the last three cards for each network and stack them at the end of the data deck. If, however, the limits are to be changed, a card of type 9., with NNCUES set to zero and MORE set to any non-zero value, is placed after the last card of type 11. The program then starts over at the beginning; consequently, the complete data deck must be repeated with the desired changes.

Figures A-1 through A-7 list the Fortran Source Statements for the programs.

```
E176  LOU FARBER        1  NB          FORTRAN SOURCE LIST       E176      06/21/67
      ISN       SOURCE STATEMENT

        0 $IBFTC E176    REF
          C      PROGRAM E176  BANDPASS FILTER DESIGN FOR ERC MICROWAVE INTEGRATED
          C      CIRCUIT STUDY --- PROGRAM WRITTEN BY ROGER ZIPOY
          C      USE OF MITE SUBROUTINE TO OPTIMIZE NETWORK --AN IMPROVEMENT OF THE
          C      SPIDER ROUTINE BOTH ROUTINES BY MIKE OHAGANS MANGMT SYSTEMS GROUP
        1        COMMON P(100),X0(40),X1(40),DX(40),Y0,Y1,REDUCE,SPEED,SMOOTH,GROW
        2        COMMON BL,KIT,KMAX,KRMAX,ISW,KFIN,KNOTE,INDEX,N,NOROT
        3        COMMON/LIMIT/NCUE(20),YZL(20),YZU(20),BLL(20),BLU(20),NNCUES,NF
        4        COMMON/ADMIT/YINR(15),YINI(15),YOUTR(15),YOUTI(15),F(90),A(90),B(9
                10),C(90),D(90),REFQ,SLOPE
        5        COMMON/GRAPH/NFP,FHIP,FLOP
        6        COMMON/COUNT/NFCNS,NFCNS2
        7        COMMON/PSSBND/FFMIN,FFMAX,G(100)
       10        DIMENSION ICUE(7),TYPE(7,7),XYL(7),XYU(7),XBL(7),XBU(7),XTYPE(10,7
                1),SPACE(40),FF(15),RUN(10),FOUT(10)
          C
          C      FIRST READ THE ADMITTANCE DATA AND FIT TO LEAST SQUARES CURVE
          C
       11     10 READ(5,100) NDATA,(RUN(I),I=1,10)
       17    100 FORMAT(I5,15X,10A6)
       20        WRITE(6,118) (RUN(I),I=1,10)
       25    118 FORMAT(////////////////////40X,41H THE FOLLOWING NETWORKS ARE DESI
                1GNED FOR //30X,10A6)
       26        DO 20 I = 1,NDATA
       27        READ(5,101)FF(I),YINR(I),YINI(I),YOUTR(I),YOUTI(I)
       30     20 F(I) =FF(I)
       32        CALL YQTN(NDATA,1)
       33        WRITE(6,107)
       34    107 FORMAT(27H1ADMITANCES ARE AS FOLLOWS //9X,1HF,4X,4HYINR,3X,11HFIT
                1TO YINR,3X,4HYINI,2X,11HFIT TO YINI,2X,5HYOUTR,2X,12HFIT TO YOUTR,
                23X,5HYOUTI,2X,12HFIT TO YOUTI //)
       35    101 FORMAT(8F10.0)
       36        DO 30 I = 1,NDATA
       37     30 WRITE(6,108)FF(I),YINR(I),A(I),YINI(I),B(I),YOUTR(I),C(I),YOUTI(I)
                1,D(I)
       41    108 FORMAT(9F10.2)
          C
          C      NEXT READ THE LINE SECTION CUE NO.,TYPE,AND LIMITS. CUE NUMBERS
          C      ARE FIXED AS FOLLOWS-- 1=2=3=SERIES SECTIONS,4=SHORTED STUB,
          C        5=OPEN STUB,6=SHUNT CAPACITOR WITH Y0 = C,BL=R,7=SERIES
          C        CAPACITOR WITH Y0=C,BL=R
       42        DO 40 I =1,7
       43     40 READ(5,102)ICUE(I),(TYPE(I,J),J=1,7),XYL(I),XYU(I),XBL(I),XBU(I)
       51    102 FORMAT(I5,7A5 ,4E10.0)
          C
          C      NOW READ THE DATA FOR MITE OPERATION
       52        READ(5,103) KMAX,KRMAX,ISW,INDEX,REDUCE,SPEED,SMOOTH,GROW,BL
       57    103 FORMAT(4I5,6E10.0)
          C
          C      NOW READ THE NO. OF FREQUECIES USED IN EVALUATION OF MERIT FTN-NFQ
          C        AND THE NO. OF FREQUENCIES USED IN PLOT-NFP,THE REFERENCE
          C        FREQUENCY--REFQ,THE LOW AND HIGH FREQUENCIES OF EVALUATION
          C        INTERVAL-FLOQ,FHIQ,AND THE LOW AND HIGH FREQ.OF THE PLOT
          C        INTERVAL-FLOP,FHIP
          C
```

Figure A-1. Fortran Source Statement - Program E 176 (Sheet 1)

```
E176  LOU FARBER        1  NB          FORTRAN SOURCE LIST       E176      06/21/67
      ISN       SOURCE STATEMENT

       60       READ(5,104)NFQ,NFP,REFQ,FLOQ,FHIQ,FLOP,FHIP,SLOPE
       63   104 FORMAT(2I5,7E10.0)
            C
            C     NFIN,NFOUT = NUMBER OF FREQUENCIES INSIDE, OUTSIDE THE PASSBAND
            C        ( NFIN + NFOUT = NFQ )
            C
            C     FOUT(I) = THE FREQUENCIES OUTSIDE THE PASSBAND
            C     FMIN AND FMAX ARE THE LOWEST AND THE HIGHEST FREQUENCIES IN THE
            C       PASS BAND, RESPECTIVELY
            C
       64       READ(5,104) NFIN,NFOUT,FMIN,FMAX
       67       READ(5,101) (FOUT(I),I=1,NFOUT)
       74       NFQ = NFIN + NFOUT
       75       FFMAX=FMAX*0.017453292/REFQ
       76       FFMIN=FMIN*0.017453292/REFQ
            C
            C     PT1 = DESIRED GAIN AT FLOQ
            C     PT2 = DESIRED GAIN IN THE PASSBAND
            C     PT3 = DESIRED GAIN AT FHIQ
            C
       77       READ(5,99) PT1,PT2,PT3
      100    99 FORMAT(15F5.0)
      101       SL1 = (PT2-PT1)/(FMIN-FLOQ)
      102       SL2 = (PT3-PT2)/(FHIQ-FMAX)
            C
            C      NOW READ THE NO.OF FILTER ELEMENTS-NNCUES,THE CODE FOR MORE
            C       DATA-MORE,AND THE THE CODE FOR THE LINE DIMENSION-KCODE
            C     NTRL = NUMBER OF RANDOM STARTING POINTS TO BE USED
            C     IF NTRL = 0, THE STARTING POINT IS DETERMINED BY XMULT  (NEXT CARD)
            C     IF NTRL IS NONZERO, XMULT IS CHOSEN RANDOMLY
            C
      103       READ(5,105)NNCUES,MORE,KCODE,NOROT ,NTRL
      111   105 FORMAT(16I5)
      112       READ(5,101) XMULT
      113       IF(NNCUES .EQ. 0) GO TO 90
      116    45 CALL LINWID(X0,REFQ,SPACE,NNCUES,1,KCODE)
            C
            C      NOW READ THE THE ELEMENT CONFIGURATION AND SORT LIMITS,SET UP
            C       THE FREQUENCIES AND GO.
            C
      117       READ(5,105)(NCUE(I),I=1,NNCUES)
      124       WRITE(6,106) NNCUES
      125   106 FORMAT(10HOTHERE ARE,I3,20H ELEMENTS AS FOLLOWS /)
      126       DO 50 I = 1,NNCUES
      127       DO 50 J = 1,7
      130       IF(NCUE(I) .EQ. ICUE(J)) GO TO 52
      133       GO TO 50
      134    52 DO 54 K = 1,7
      135    54 XTYPE(I,K) = TYPE(J,K)
      137       YZL(I) = XYL(J)
      140       YZU(I) = XYU(J)
      141       BLL(I) = XBL(J)
      142       BLU(I) = XBU(J)
      143    50 CONTINUE
      146       WRITE(6,117)
```

Figure A-1. Fortran Source Statement - Program E 176 (Sheet 2)

```
F176  LOU FARBER        1  NB          FORTRAN SOURCE LIST       E176      06/21/67
      ISN       SOURCE STATEMENT

      147   117 FORMAT(9X,12H ELEMENT NO.,10X,4HTYPE,28X,6HLIMITS /)
      150       DO 60 I = 1,NNCUES
      151    60 WRITE(6,109) I,(XTYPE(I,J),J=1,7), YZL(I),YZU(I),BLL(I),BLU(I)
      157   109 FORMAT(10X,I5,5X,7A5,4F10.2)
      160       N= 2*NNCUES
          C
          C
      161       DO 89 IDUM = 1,NTRL
      162    61 CONTINUE
      163       XK = 0.0
      164       XFIN= NFIN
      165       XJ = 0.0
      166       NOUT = NFOUT/2
      167       FINTVL = FMAX-FMIN
      170       J = 0
      171       DO 70 I=1,NFQ
      172       XI = I
      173       IF(I.GT.NOUT) GO TO 170
      176       G(I) = SL1*(FOUT(I)-FMIN) + PT2
      177       F(I) = FOUT(I)
      200       J = J + 1
      201       GO TO 70
      202   170 ITEST = NFIN + NOUT
      203       IF(I.GT.ITEST) GO TO 171
      206       XK = XK + 1.0
      207       F(I) = FMIN + FINTVL*(XK-1.0)/(XFIN-1.0)
      210       G(I) = PT2
      211       GO TO 70
      212   171 XJ = XJ + 1.0
      213       J = J + 1
      214       F(I) = FOUT(J)
      215       G(I) = SL2*(FOUT(J)-FMAX) + PT2
      216    70 CONTINUE
      220       CALL YQTN(NFQ,2)
      221       NF = NFQ
      222       DO 71 K = 1,N,2
      223       KK = (K + 1)/2
      224       DX(K) = (YZU(KK) - YZL(KK))
      225    71 DX(K+1) = (BLU(KK) - BLL(KK))
      227       IF(NTRL.NE.0) XMULT = RANDOM(DUM)
      232    72 DO 73 K = 1,N,2
      233       KK = (K + 1)/2
      234       X0(K) = YZL(KK) + DX(K)*XMULT
      235    73 X0(K+1) =  BLL(KK) + DX(K+1)*XMULT
      237    79 WRITE(6,110)
      240   110 FORMAT(//33H1THE STARTING VALUES ARE FOLLOWS //3X,8H ELEMENT,6X,
                 12HYZ,8X,2HBL /)
      241       DO 80 I = 1,N,2
      242       JJ = (I+1)/2
      243    80 WRITE(6,111) JJ,X0(I),X0(I+1)
      245   111 FORMAT(I10,4F10.1)
      246       NFCNS = 0
      247       CALL MITE
      250       WRITE(6,112)
      251   112 FORMAT(//49H THE FINAL VALUES OF THE VARIABLES ARE AS FOLLOWS //3X
```

Figure A-1. Fortran Source Statement - Program E 176 (Sheet 3)

```
E176  LOU FARBER        1  NB            FORTRAN SOURCE LIST        E176      06/21/67
      ISN       SOURCE STATEMENT

               1,8H ELEMENT,12X,4HTYPE,25X,2HYZ,8X,2HBL,5X,5HWIDTH,5X,6HLENGTH /)
          252       CALL LINWID(XO,REFQ,SPACE,NNCUES,2,KCODE)
          253       DO 130 I = 1,N,2
          254       JJ = (I+1)/2
          255   130 WRITE(6,119)JJ,(XTYPE(JJ,K),K=1,7),XO(I),XO(I+1),SPACE(I),SPACE(I+
                   11)
          263       WRITE(6,113) REFQ
          264   113 FORMAT(/27H THE REFERENCE FREQUENCY IS,F5.2,10H GIGAHERTZ)
          265       WRITE(6,114) YO
          266   114 FORMAT(//37H FINAL VALUE OF THE MERIT FUNCTION = ,1PE15.6/)
          267       GO TO (140,141,142),KFIN
          270   140 CALL BCI(EXIT,6HERROR )
          271       GO TO 143
          272   141 CALL BCI(EXIT,6H MAX  )
          273       GO TO 143
          274   142 CALL BCI(EXIT,6H MIN  )
          275   143 CONTINUE
          276       WRITE(6,115) EXIT
          277   115 FORMAT(1H1,1X ,A6,30H IS THE REASON FOR MITE RETURN )
          300       WRITE(6,116) KIT,NFCNS
          301   116 FORMAT( 43H THIS AMAZING FEAT HAS BEEN ACCOMPLISHED IN,I4,11H ITER
                   1ATIONS,/ I5,38H EVALUATIONS OF EVAL HAVE TAKEN PLACE. /)
          302       CALL SSRC(XO,YO,3)
          303    89 CONTINUE
          305       READ(5,105)NNCUES,MORE,KCODE,NOROT ,NTRL
          313       READ(5,101) XMULT
          314       IF(NNCUES .GT. 0) GO TO 150
          317    90 IF(MORE .EQ. 0) GO TO 160
                C
                C     MORE GREATER THAN 0 MEANS ANOTHER SET OF DATA
                C
          322       GO TO 10
          323   150 DO 151 I = 1,NDATA
          324   151 F(I) = FF(I)
          326       CALL YOTN(NDATA,2)
          327       WRITE(6,107)
          330       DO 152 I = 1,NDATA
          331   152 WRITE(6,108)FF(I),YINR(I),A(I),YINI(I),B(I),YOUTR(I),C(I),YOUTI(I)
                   1,D(I)
          333       GO TO 45
          334   119 FORMAT(I10,7A5,4F10.1)
          335   160 STOP
          336       END
```

Figure A-1. Fortran Source Statement - Program E 176 (Sheet 4)

```
E176  LOU FARBER        1  NB          FORTRAN SOURCE LIST        SSRC      06/21/67
      ISN       SOURCE STATEMENT

        0 $IBFTC SSRC
        1       SUBROUTINE SSRC(X,VAL,KK)
        2       COMPLEX DUM,DUM1,DUM2,DUM3
        3       DIMENSION X(1),RC(90),YCR(90),YCI(90),DB(90)
        4       COMMON/LIMIT/NCUE(20),YZL(20),YZU(20),BLL(20),BLU(20),NNCUES,NF
        5       COMMON/ADMIT/YINR(15),YINI(15),YOUTR(15),YOUTI(15),F(90),A(90),B(9
               10),C(90),D(90),REFQ,SLOPE
        6       COMMON/GRAPH/NFP,FHIP,FLOP
        7       COMMON/PSSBND/FFMIN,FFMAX,G(100)
       10       GO TO (1,2,2), KK
       11     1 CONTINUE
       12       RETURN
       13     2 IF(KK .EQ. 3) GO TO 70
       16       GO TO 71
       17    70 WRITE(6,110)
       20       NF=NFP
       21       XNF = NFP
       22       FINTVL = FHIP - FLOP
       23       DO 72 I = 1,NFP
       24       XI = I
       25       F(I) = FLOP + FINTVL*(XI-1.)/(XNF - 1.)
       26    72 CONTINUE
       30       CALL YQTN(NFP,2)
       31   110 FORMAT(9X,1HF,9X, 9HYOUTR FIT,7X, 9HYOUTI FIT,9X, 3HYCR,11X,3HYCI,
              111X,6HXTRLOS,9X,6HS11**2,10X,4HSUM / )
       32    71 SUM = 999999.
       33        VAL = SUM
       34       DO 40 I = 1,NNCUES
       35       J = 2 * I
       36       JJ = J - 1
       37       IF(X(JJ) .LT. YZL(I) .OR. X(JJ) .GT. YZU(I)) GO TO 30
       42    40 IF(X(J) .LT. BLL(I) .OR. X(J) .GT. BLU(I)) GO TO 30
       46       DO 10 I = 1,NF
       47       YCR(I) = A(I)
       50    10 YCI(I) = B(I)
       52       DO 11 M = 1,NNCUES
       53       NDUM = NCUE(M)
       54       I = 2*M - 1
       55       GO TO(12,12,12,13,14,21,22),NDUM
       56    12 DO 15 K = 1,NF
       57       T = TAN( X(I + 1) * F(K))
       60       YNUMR = X(I) * YCR(K)
       61       YNUMI = X(I) * (YCI(K) + X(I) * T)
       62       DUM = CMPLX(YNUMR,YNUMI)
       63       YDENR = X(I) - YCI(K) * T
       64       YDENI = YCR(K) * T
       65       DUM1 = CMPLX(YDENR,YDENI)
       66       DUM  =  DUM/DUM1
       67       YCR(K) =            REAL(DUM)
       70    15 YCI(K) =            AIMAG(DUM)
       72       GO TO 11
       73    13 DO 16 K = 1,NF
       74       T  = - X(I) / TAN(X(I + 1) * F(K))
       75    16 YCI(K) =  YCI(K) + T
       77       GO TO 11
```

Figure A-2. Subroutine for Evaluating SSRC (Sheet 1)

```
F176  LOU FARBER        1  NB          FORTRAN SOURCE LIST       SSRC      06/21/67
      ISN       SOURCE STATEMENT

      100     14 DO 17 K = 1,NF
      101        T = X(I)*TAN(X(I+1)*F(K))
      102     17 YCI(K) = YCI(K) + T
      104        GO TO 11
      105     21 DO 23 K = 1,NF
      106        XNUM = F(K)*360.*REFQ*X(I)
      107        DEN = XNUM*X(I+1)/3000.
      110        DEN = DEN*DEN
      111        DEN = 1. + DEN
      112        T = XNUM/DEN
      113        YCI(K) = YCI(K) + T
      114        T = T*XNUM*X(I+1)/3000.
      115     23 YCR(K) = YCR(K) + T
      117        GO TO 11
      120     22 DO 24 K = 1,NF
      121        YR = YCR(K)*.001
      122        YI = YCI(K)*.001
      123        DEN = YR*YR + YI*YI
      124        ZR = YR/DEN
      125        ZI = -YI/DEN
      126        ZR = ZR + X(I+1)*.666666667
      127        ZI = ZI - 1000./(F(K)*360.*REFQ*X(I))
      130        DEN = ZR*ZR + ZI*ZI
      131        YCR(K) = 1000.*ZR/DEN
      132     24 YCI(K) = -1000.*ZI/DEN
      134        GO TO 11
      135     11 CONTINUE
      137         VAL = 0.0
      140        SUM = 0.
      141        DO 50 I = 1,NF
      142        YNUMR = C(I) - YCR(I)
      143        YDENR = C(I) + YCR(I)
      144        YNUMI = D(I) - YCI(I)
      145        YDENI = D(I) - YCI(I)
      146        DUM = CMPLX(YNUMR,YNUMI)
      147        DUM1 = CMPLX(YDENR,YDENI)
      150        DUM = DUM / DUM1
      151        XX = REAL(DUM)
      152        YY = AIMAG(DUM)
      153        RCS = XX * XX + YY * YY
      154        FG = 1. - RCS
      155        IF(FG .LT. 1.E-10)  FG = 1.0E-10
      160        FGDB = 10.*ALOG10(FG)
      161        DELF = REFQ*(F(I)/.017453292 - 1.)
      162        XTRLOS = SLOPE*DELF
      163        GAIN = XTRLOS - FGDB
      164        AGAIN = ABS(GAIN)
      165        SUM = SUM + AGAIN
      166         TEMP = AGAIN - G(I)
      167         TEMP = ABS(TEMP)
      170        VAL = VAL + TEMP
      171        IF(KK .EQ. 3) GO TO 60
      174        GO TO 50
      175     60 F(I)= F(I) * REFQ/0.017453292
      176        WRITE(6,111) F(I),C(I),D(I),YCR(I),YCI(I),XTRLOS,RCS,SUM
```

Figure A-2. Subroutine for Evaluating SSRC (Sheet 2)

```
F176  LOU FARBER        1  NB          FORTRAN SOURCE LIST        SSRC      06/21/67
      ISN       SOURCE STATEMENT

      177           DB(I) = GAIN
      200        50 CONTINUE
      202           IF(KK.LT.3) GO TO 31
      205        30 VAL=SUM
      206        31 CONTINUE
      207           IF(KK .EQ. 3) CALL PLOTRC(F,DB,NF)
      212           RETURN
      213       111 FORMAT(8E15.6)
      214           END
```

Figure A-2. Subroutine for Evaluating SSRC (Sheet 3)

APPENDIX B

TEST PLAN

S-BAND TELEMETRY TRANSMITTER BREADBOARD

APPENDIX B

TEST PLAN

A. SCOPE

1. This plan is to be used for testing the ERC breadboard transmitter.

2. The specifications to which the transmitter will be tested are as follows:

   a. Frequency - 2.2 - 2.3 GHz

   b. Frequency Stability - ±0.5% without AFC

   c. Efficiency - 10 - 20% dc to RF

   d. Power Output - 1.0 watts min.

   e. Modulation:

      (1) Type - FM

      (2) Baseband - 2 kHz to 1 MHz

      (3) Deviation - ± 1.5 MHz

      (4) Sensitivity - 0.2V RMS/100 kHz

      (5) Linearity - 1.0%

   f. Input Impedance - 600 ohms

B. TEST EQUIPMENT

The following test equipment or its equivalent is required to evaluate the transmitter performance.

Power supply

73 ohm to 50 ohm impedance transformer - Microlab PI-30P

20 dB directional coupler - HP777D - 2 ea.

10 dB PAD - Weinschel 530A-10

20 dB PAD - Weinschel 530A-20

Precision variable attenuator - ARRA #4414-40

50 ohm termination - HP908A

Power meter - HP 431B

Counter - HP 5245 L

Frequency converter - HP 5254A

Voltmeter ac - HP 400E

Spectrum analyzer plug-in - Tektronix 1L20

Ammeter - HP 428B

Test oscillator - HP 651A

Temperature Chamber

Signal Generator - HP8614A

TWT Amplifier - HP941C

Noise Generator

Transfer Oscillator

FM Receiver

C. TESTS

Where applicable, MIL-STD-449C will be used as a guide.

1. Size and Weight

The Transmitter will be measured along its three axes and weighed to verify that its physical parameters are within the prescribed limits.

2. Center Frequency and Frequency Stability

With the equipment connected as shown in Figure B-1, and -24.5 volts dc applied, the modulation input is shorted and the center frequency is measured with the electronic counter. The transmitter is allowed to operate for 30 minutes and the center frequency drift is monitored with the counter. The center frequency must fall between 2.2 and 2.3 GHz and must be stable within ±0.5 percent. Detailed steps are as follows:

Connect the equipment as shown in Figure B-1.

Short the modulation input of the transmitter

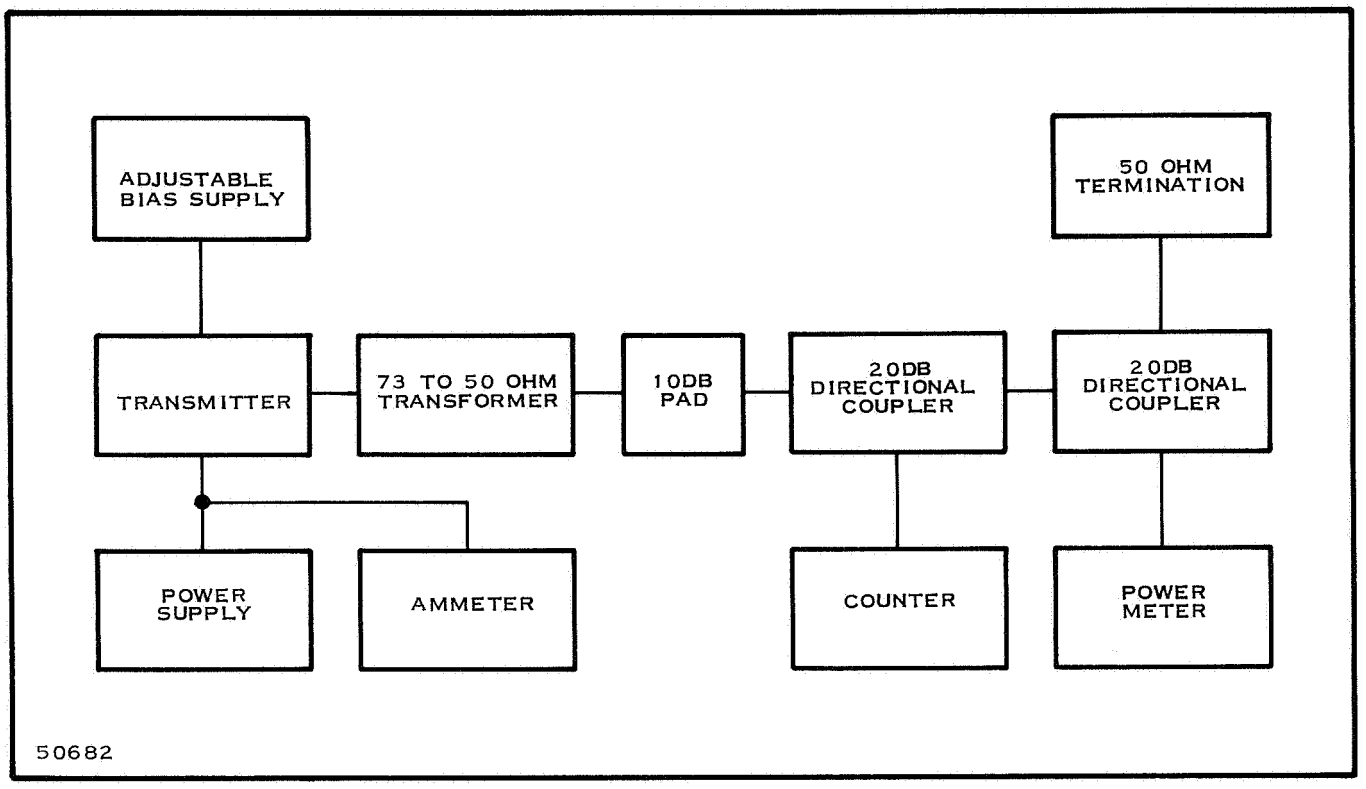

Figure B-1. Power Output Versus Frequency Test Circuit

Apply -24.5 volts dc

Allow 5 minutes warmup period

After 5 minute warmup read the frequency shown on the HP 5245L counter and record

Verify that the frequency does not vary more than ±0.5 percent in a 30-minute time period.

3. Power Output Versus Frequency

This test is to determine how the transmitter output power varies as its frequency is varied. In order to vary the transmitter frequency in a known manner, the modulation input will be shorted, preventing any unwanted external signal from deviating the carrier, and the varactor diode capacitance will be varied by applying an adjustable bias voltage to it from an external power supply. The varactor voltage will be changed in such a manner as to change the output frequency in 10-MHz steps from 2.2 - 2.3 GHz. The output power will be monitored by a power meter and will be recorded from 2.2 - 2.3 GHz in 10-MHz steps. The output frequency will be monitored by a counter. The test circuit diagram is shown in Figure B-1.

With the equipment connected as shown in Figure B-1 and with -24 volts dc applied, the modulation input is shorted and the power meter indication is read. This power level is referred to the transmitter output, taking into account the insertion loss and coupling between the power meter and the transmitter. The power level referred to the transmitter must be 1.0 watt, minimum. Detailed steps are as follows:

Connect the equipment as shown in Figure B-1

Short the modulation input

Apply -24.5 volts dc

Record the power meter reading and verify 1.0-watt minimum transmitter output

4. Efficiency

With the equipment connected as shown in Figure B-1 and with -24.5 volts dc applied, the modulation input is shorted and the ammeter and power meter are read. The dc to RF efficiency is calculated from

$$\text{Percent EFF} = \frac{P_{out} \times 100}{24.5 \times I}$$

The efficiency must be greater than 10 percent. Detailed test steps are as follows:

Connect the equipment as shown in Figure B-1

Short the modulation input

Apply -24.5 volts dc

Record the ammeter reading in amps

Record the power meter reading in watts

Determine the dc to RF efficiency

$$\text{Percent EFFICIENCY} = \frac{P_{watts} \times 100}{24.5 \times I_{amperes}}$$

Verify this calculation of efficiency to be greater than 10 percent.

5. Modulation Characteristics

This test is to determine the modulation characteristics at 2.2 and 2.3 GHz. The modulation frequency response, deviation linearity, and deviation sensitivity will be measured at 2.2 and 2.3 GHz, using the methods called out below:

a. Modulation Frequency Response

The equipment is connected as shown in Figure B-2. In checking the modulation frequency response a constant deviation - 300 kHz-is selected and the modulation voltage is measured at various input modulation frequencies. To measure the deviation, a spectrum analyzer is used, employing the Crosby Zero Method (the carrier amplitude goes to zero at certain modulation indices). Using the relationship

$$M = \Delta f / f_m$$

where

M = the modulation index

Δf = the peak deviation, and

f_m = the modulating frequency

the deviation can be accurately set and the amplitude of the modulating signal can be measured. At modulation indices lower than 2.4048, the carrier amplitude does not go to zero. However, the amplitude of the carrier may be set to a preselected point determined by the modulation index selected, and the deviation can be calculated using the $J_0(M)$ Bessel function. Detailed steps for determining the frequency response are as follow:

(1) Connect the equipment as shown in Figure B-2.

(2) Short the modulation input.

(3) Apply -24.5 volts dc to the transmitter.

(4) Set the variable attenuator setting to zero.

(5) Set the carrier amplitude displayed on the spectrum analyzer to full scale on the linear display.

(6) Set the variable attenuator for 0.2-dB attenuation.

(7) Mark the amplitude peak of the carrier on the spectrum analyzer display for the 0.20-dB setting of (6).

(8) Repeat (6) and (7) for an attenuator setting of 0.8 dB.

(9) Repeat (6) and (7) for an attenuator setting of 2.33 dB.

(10) Remove the short from the modulation input and connect the test oscillator.

(11) Set the variable attenuator for zero attenuation.

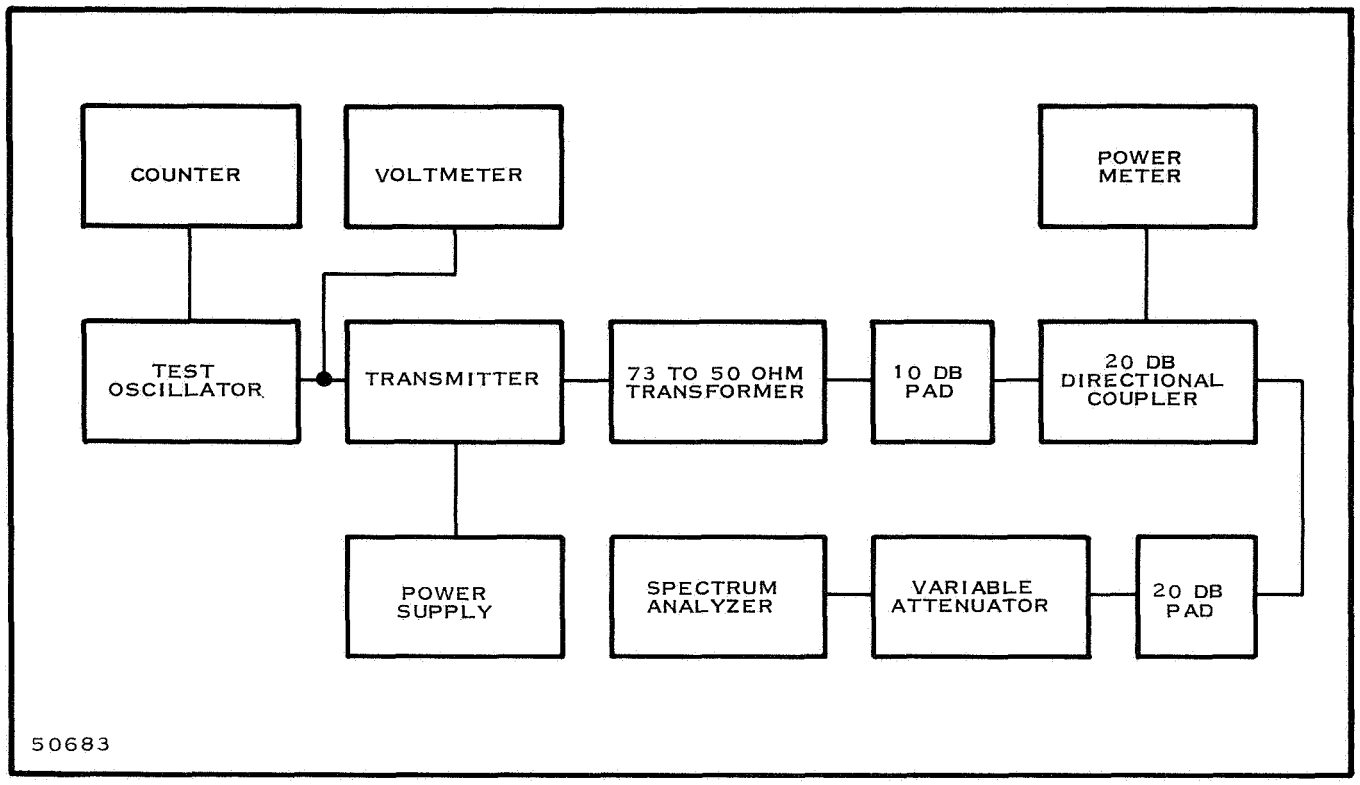

Figure B-2. Characteristics Test Circuit Modulation

(12) Set the test oscillator frequency to 1000.000 kHz..

(13) Increase the test oscillator output voltage until the carrier amplitude is reduced by 0.20 dB. [See step (7).]

(14) Record the voltage at the modulation input.

(15) Set the test oscillator frequency to 500.000 kHz.

(16) Increase the test oscillator output voltage until the carrier amplitude is reduced by 0.80 dB. [See step (8).]

(17) Record the voltage at the modulation input.

(18) Set the test oscillator frequency to 300.000 kHz..

(19) Increase the test oscillator output voltage until the carrier amplitude is reduced by 2.33 dB.[See step (9).] Record the voltage at the modulation input.

(20) Set the test oscillator frequency to 124.750 kHz. Increase the output amplitude of the test oscillator until the carrier amplitude goes to zero.

(21) Record the voltage at modulation input.

(22) Set the test oscillator to 54.347 kHz.

(23) Increase the output amplitude of the test oscillator until the carrier amplitude goes to zero for the second time. Record the voltage at the modulation input.

(24) Repeat step (20) for all values of f_m shown in Table B-1. Adjust the amplitude of the test oscillator until the carrier amplitude goes to zero the prescribed number of times as shown below.

f_m(kHz)	Order of Carrier Zero
124.750	1
54.347	2
34.667	3
25.442	4
20.093	5
16.601	6
14.143	7

(25) Plot the modulation voltage amplitude versus modulating frequency.

b. Deviation Linearity

The equipment is connected as shown in Figure B-2. In checking the linearity, a constant modulating frequency - 70.716 kHz - is used and the modulation input levels are measured at various deviations. The Crosby Zero Method is used to determine the deviation. Detailed steps for the linearity measurement are as follow:

(1) Connect the equipment as shown in Figure B-2.

(2) Apply -24.5 volts dc.

(3) Set the test oscillator frequency to 70.716 kHz.

(4) Increase the output amplitude of the test oscillator until the carrier amplitude goes to zero.

(5) Record the voltage at the modulation input.

(6) Increase the voltage from that obtained in step (4) until the carrier amplitude goes to zero for the second time.

(7) Record the voltage at the modulation input.

(8) Repeat step (6) until the carrier amplitude goes to zero for the seventh time, recording the modulation input voltage at each point that the carrier amplitude goes to zero. Listed below are the peak deviations corresponding to the order of the carrier zero.

Order of Carrier Zero	Peak Deviation (kHz)
1	170.057
2	390.359
3	611.955
4	833.847
5	1055.853
6	1277.915
7	1500.000

(9) A plot of modulation voltage versus deviation should be linear within ±1.0 percent.

c. Deviation Sensitivity

The equipment is connected as shown in Figure B-2. The deviation sensitivity is calculated using the test results of paragraph C.5.b. Detailed steps for performing the calculations are given below:

Referring to the sequence of steps for determining deviation linearity, determine the deviation sensitivity by using the results of step (8), dividing the voltages as measured in steps (5), (7) and (8) by their corresponding peak deviations. The sensitivity should measure 0.2V RMS/100 kHz.

6. Input Impedance

The equipment is connected as shown in Figure B-3. The transmitter is deviated a specified amount - 1.5 MHz - at a selected modulating frequency with, and without, a 600-ohm resistor in series with the modulation input. The amplitude of the modulating signal is measured. The input impedance of the transmitter is calculated, using the two amplitudes of the modulating signal. Detail steps for measuring the input impedance are shown below:

(1) Connect the equipment as shown in Figure B-3

(2) Apply -24.5 volts dc

(3) Set the test oscillator frequency to 623.752 kHz

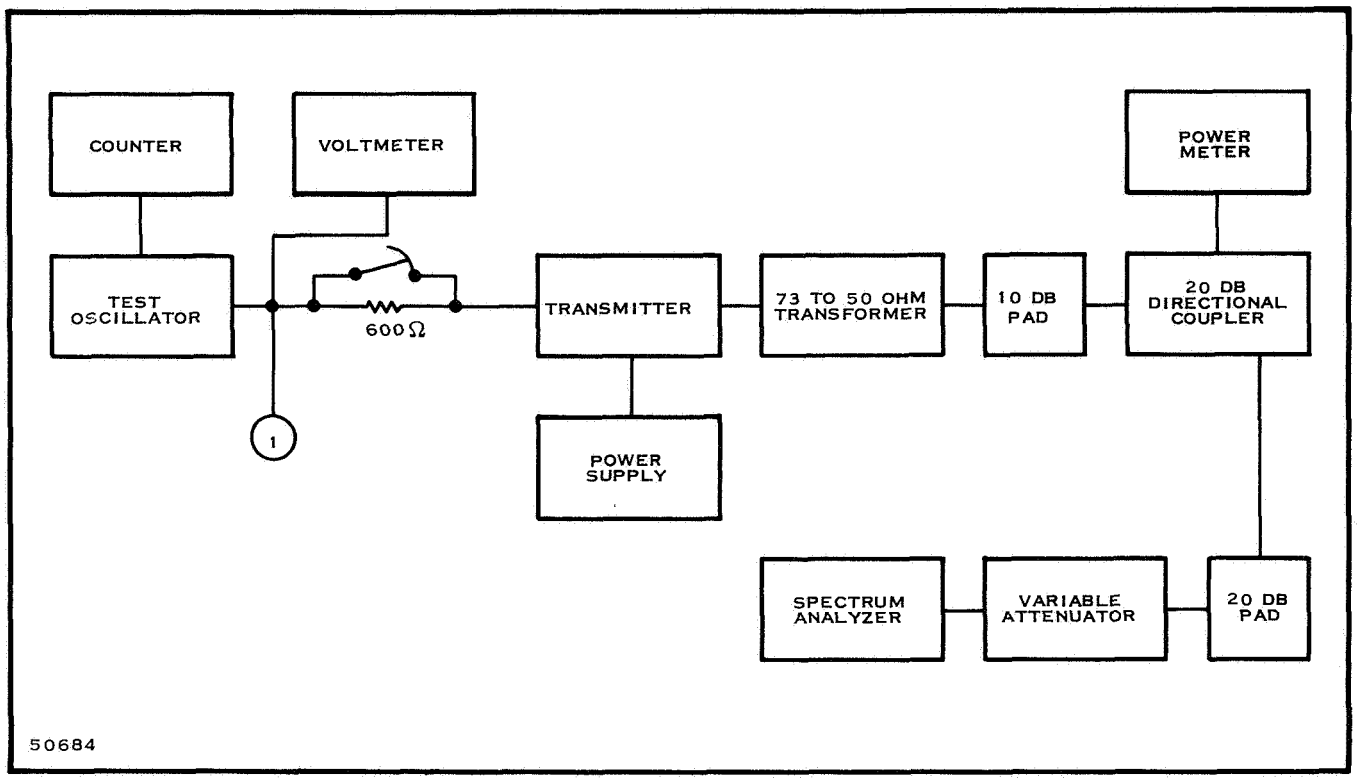

Figure B-3. Input Impedance Test Circuit

(4) Increase the output voltage amplitude of the test oscillator until the carrier amplitude goes to zero for the first time

(5) Record the voltage measured at point 1 in Figure B-3

(6) Remove the short across the 600-ohm resistor

(7) Increase the amplitude of the modulating signal until the carrier amplitude goes to zero for the first time

(8) Record the voltage measured at point 1 in Figure B-3

(9) The input impedance is

$$Z_{in} = \frac{V_{(5)} \times 600}{V_{(8)} - V_{(5)}}$$

7. Spurious Emissions

This test is to observe the frequency spectrum from the transmitter fundamental frequency f_o to some upper frequency limit, to determine if any spurious signals are present in the transmitter output. During this test the modulation input

will be shorted to prevent any external signals from modulating the carrier. The output spectrum will encompass the range from f_o to 12 GHz and will be observed on the spectrum analyzer. If any spurious signals are present their frequency and amplitude will be determined and the spectrum analyzer display will be recorded on film. Should the spectrum analyzer sensitivity prove to be insufficient, a transfer oscillator and a calibrated FM receiver can be used to detect any spurious output signals. During this test the output spectrum will be observed for f_o equal to 2.2, 2.25, and 2.3 GHz. Figure B-4 shows the block diagram for the test setup, using both the spectrum analyzer and the transfer oscillator/FM receiver configurations.

8. Sideband Splatter

Sideband splatter, as defined by MIL-STD-449C, is "those emissions that appear outside of the necessary bandwidth and which are a result of intermodulation products of the modulation spectrum." During this test two modulating frequencies within our baseband will be applied to the modulation input. The necessary bandwidth was determined to be 8 MHz. The output spectrum will be monitored outside $f_o \pm 4$ MHz for any frequency components. If a signal appears outside $f_o \pm 4$ MHz, one modulating signal will be removed to see if the signal disappears. If the signal does disappear it will be considered to be a sideband splatter signal and its frequency and amplitude will be determined and recorded on film. Cross modulation products present within the necessary bandwidth also will be recorded. The test will be performed at several modulating frequency pairs. The test circuit block diagram is shown in Figure B-5.

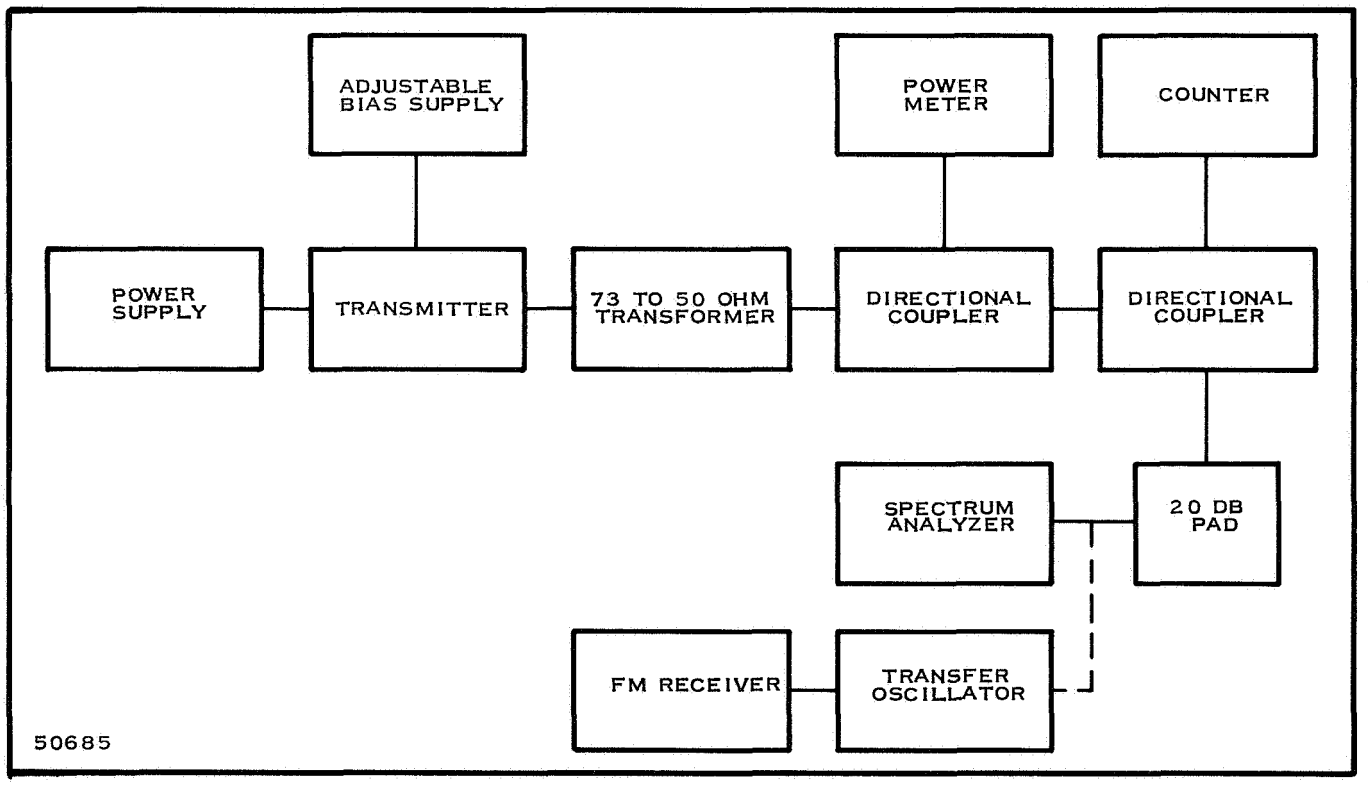

Figure B-4. Spurious Emission Test Circuit

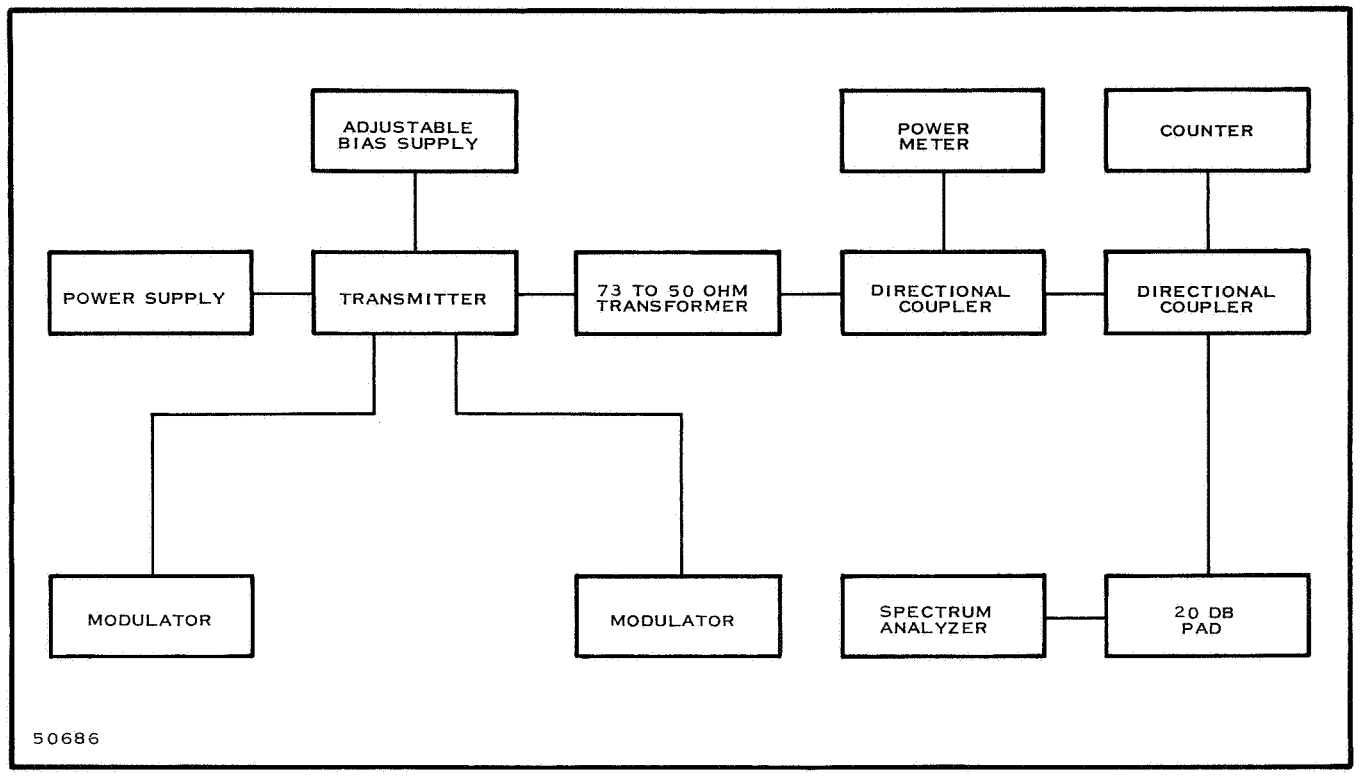

Figure B-5. Sideband Splatter Test Circuit

9. Intermodulation

This test is to determine the amount of intermodulation present when two or more transmitters have some mutual coupling between their respective output stages. In this test a signal generator output is coupled in known amounts into the output of the transmitter. The output spectrum is then observed on a spectrum analyzer for the various degrees of coupling. The spectrum analyzer will display a spectrum defined by

$$f_s = nf_o \pm mf_i$$

where

f_s = intermodulation product frequency generated

f_o = transmitter frequency

f_i = interference signal frequency

$n + m$ = order

The spectrum of interest will be confined to third- and fifth-order difference frequencies only. Intermodulation tests will be conducted at f_o equal to 2.2, 2.25, and 2.3 GHz. The test circuit block diagram is shown in Figure B-6.

10. Temperature Tests

These tests are to acquire data for the full description of the transmitter operating characteristics at temperature extremes. All modulation characteristics (frequency response, deviation sensitivity, and deviation linearity), power output versus frequency, frequency stability, spurious emissions and efficiency will be measured at f_o equal to 2.2, 2.25, and 2.3 GHz, at temperatures of -28°C and +71°C.

11. Sine Vibration

This test is to determine the transmitter operating characteristics under sinusoidal vibration. The transmitter will be vibrated along each of its axes, in accordance with MIL-STD-202C Method 204A, Test Condition C, Part 2, except that the total time to traverse the frequency range shall be four minutes. During the vibration cycles the output power and frequency spectrum will be monitored. Any sensitive frequencies observed on the spectrum analyzer during the cycle will be recorded and returned to for detailed analysis after the full cycle has been accomplished. The residual FM caused by vibration will be determined by measuring the kHz deviation. The transmitter will be tested immediately before and after the vibration test by measuring the power output and modulation characteristics. The block diagram for the vibration test is shown in Figure B-7.

12. Random Vibration

This test is to determine the transmitter's ability to withstand random vibration of a prescribed amount. The transmitter will be vibrated for two minutes, along each of its three axes, from 20 to 2000 Hz, at $2g^2/Hz$, 20g rms. The output power will be monitored. Since it would be impossible to determine the exact frequency of vibration, the spectrum analyzer will be used only for observation. The transmitter modulation and power output characteristics will be measured immediately before and after the random vibration tests. The test circuit block diagram is shown in Figure B-7.

13. Shock

This test is to determine the transmitter's ability to withstand shock. The transmitter will be subjected to a shock of 30g, 11 milliseconds duration, along each of its three axes. During shock, the output power and frequency spectrum will be monitored. Prior to and immediately after the shock test the transmitter modulation and power output characteristics will be measured.

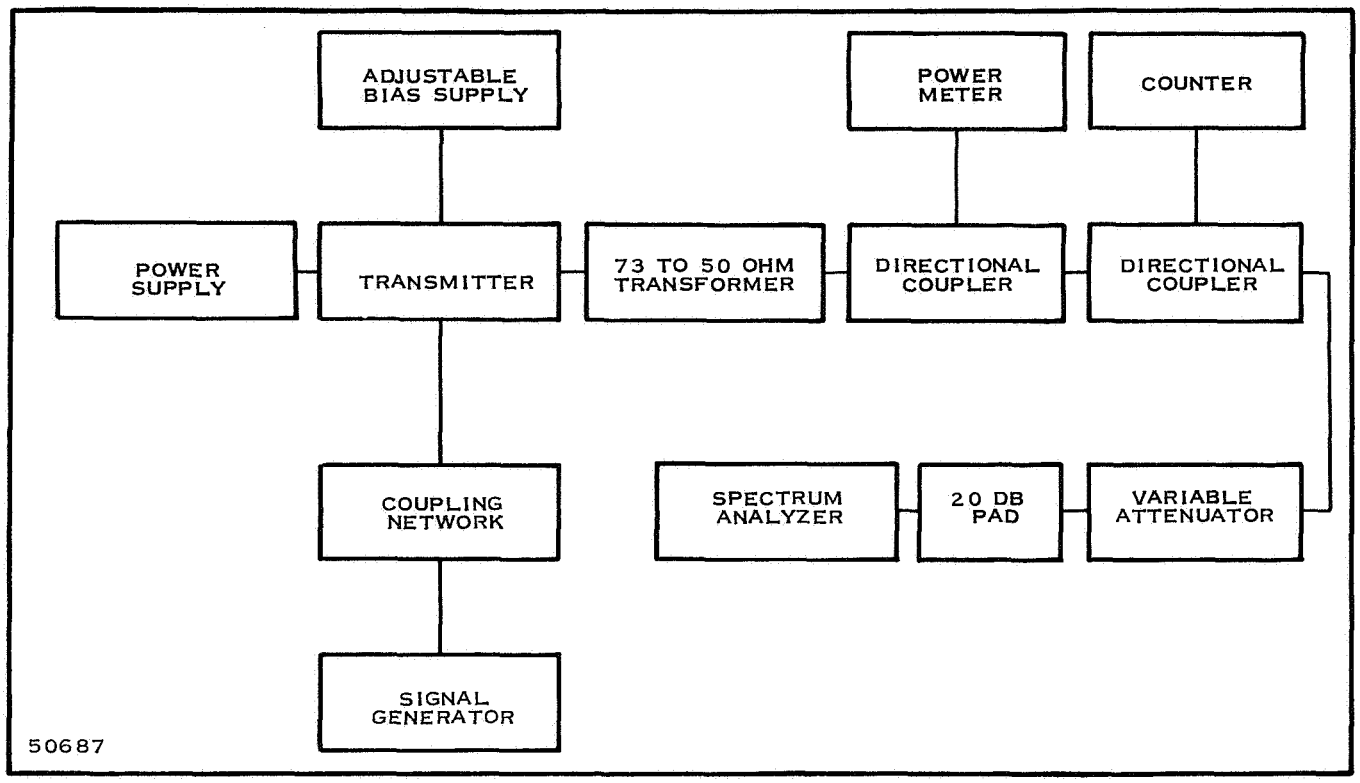

Figure B-6. Intermodulation Test Circuit

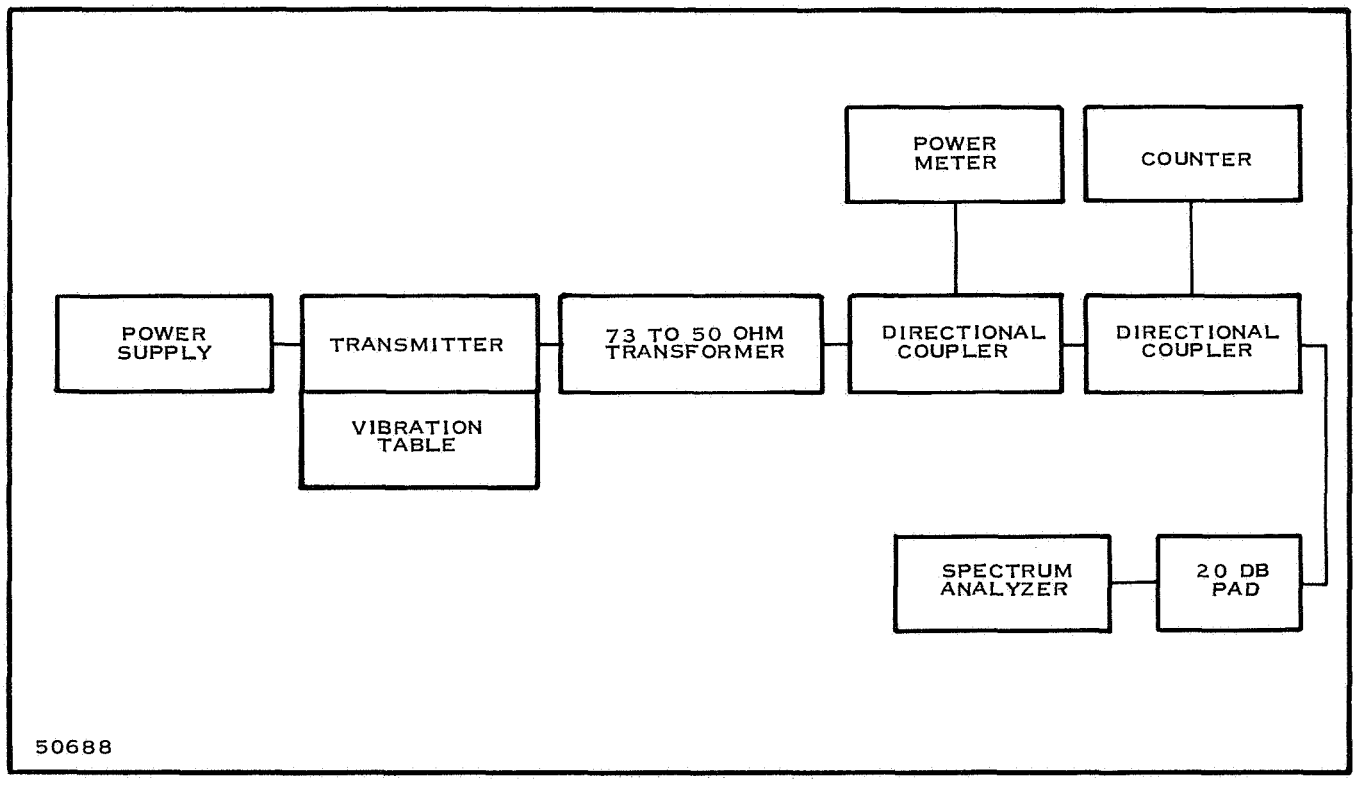

Figure B-7. Vibration Test Circuit